Hardware Memo 2

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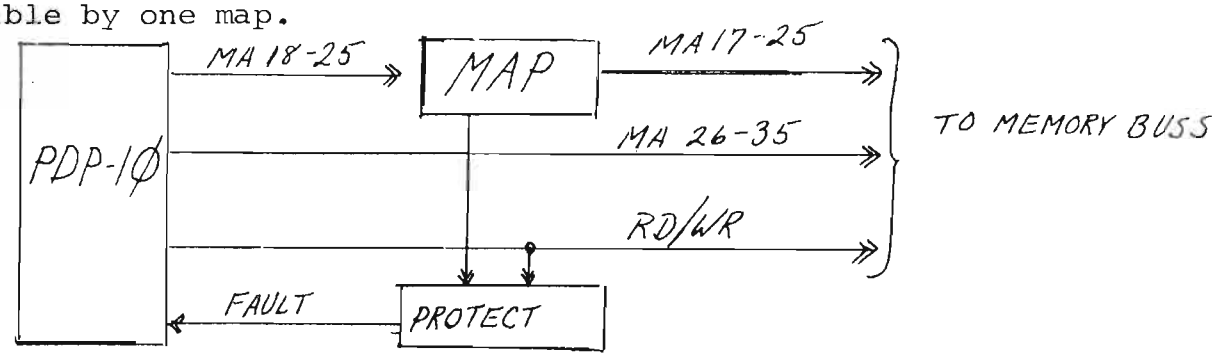
PDP-1Ø Paging Device

2/20/70

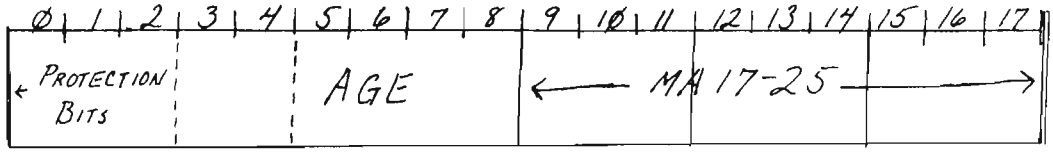
1.0 PAGING

The MAC-1Ø Paging Device is a hardware device inserted between the PDP-1Ø processor and its memory buss. It maps address data from the processor (virtual address) into an address sent to the memory system (absolute address). Virtual and absolute memory space is divided into pages, each 1Ø24 words long. Virtual MA 18-25 are taken as the page number input to the paging box. The output consists of MA bits 17-25 mapped by the paging transformation, with MA 26-35 passed unmodified. Although the resulting address spans 512K of core, only up to 256K are addressable by one map.



2.0 PAGE WORDS

The mapping information is stored in core memory in page tables. A page table consists of up to 128 18-bit entries called page words.



Ø-1 - Protection bits -

ØØ - Not Accessable

Ø1 - Read Only, executable by Pure code

1Ø - Read/Write/First

(Similar to Read Only, but not executable by Pure code)

2-4 - Unused

5-8 - Age - set from the Age register every time page word referenced.

9-17 - The absolute page number that this virtual page is mapped into.

2.1 DBR

The map contains three Descriptor Base Registers, which point to page tables. DBR1 maps the 128 pages in the lower half (Ø-377,777) of USER virtual memory. DBR2 maps the upper 128 pages 4ØØ,ØØØ-777,777) of USER memory. DBR3 maps the upper 128 pages of EXEC memory (4ØØ,ØØØ-777,777). EXEC addresses below 4ØØ,ØØØ are not mapped.

2.2 PAGE TABLES

The page table is addressed at its base by the corresponding DBR. Even page numbers are stored in the left halfword, in increasing addresses within the table. The maximum length of a page table is specified by a DBR length (DBRL) register associated with each DBR. The DBRL contains the number of full words in the page table (Ø-64).

2.3 ASSOCIATIVE REGISTERS

Each time an entry in a page table is referenced to determine the mapping and protection information, bits Ø, 1, 9-17 of the page

word are stored in an associative register (AR), keyed by the virtual page number plus a bit for USER versus EXEC pages. If another reference occurs to the same virtual page, the necessary information will be found in the AR, without reference to the page table in memory. The main group of associative registers. is called the A memory and consists of sixteen independent AR's. A four-bit counter (RBC) determines which AR is to be stored into when a new page table reference is made. The counter advances after each refill and acts like a ring buffer pointer.

2.3.1 B AND C MEMORIES

In addition to the A memory, two more groups of sixteen AR's, called the B and C memories exist. These are keyed by a single five-bit key for each of the sixteen AR's. The key selects USER/EXEC pages, and associates a sixteen-page block of virtual memory. A contiguous 16K of virtual memory is mapped into sixteen separate pages.

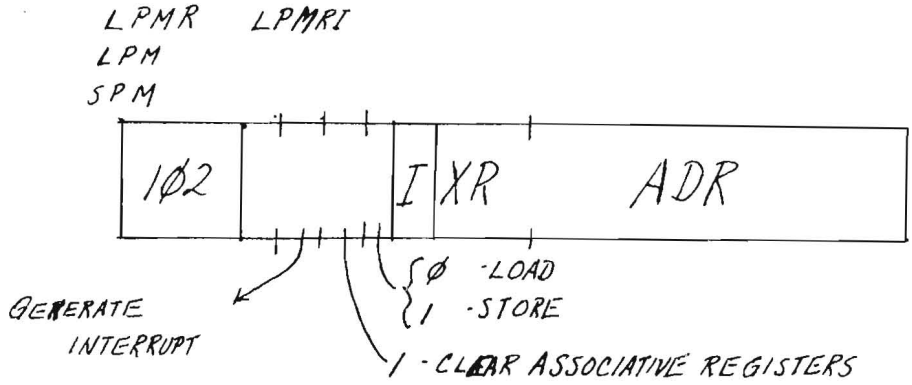
The effect of this is invisible to the mapping process. The addition of the B and C memories merely diverts page refills for a specific area of virtual memory. They might be used to shade the A memory from the addresses generated by the instruction fetches or reference to a group of data tables. Since the A, B, and C memories provide 48K of mapping information contained in hardware associative registers, only programs with unusually

large working sets need incur any overhead referencing the page tables.

2.4 AGING

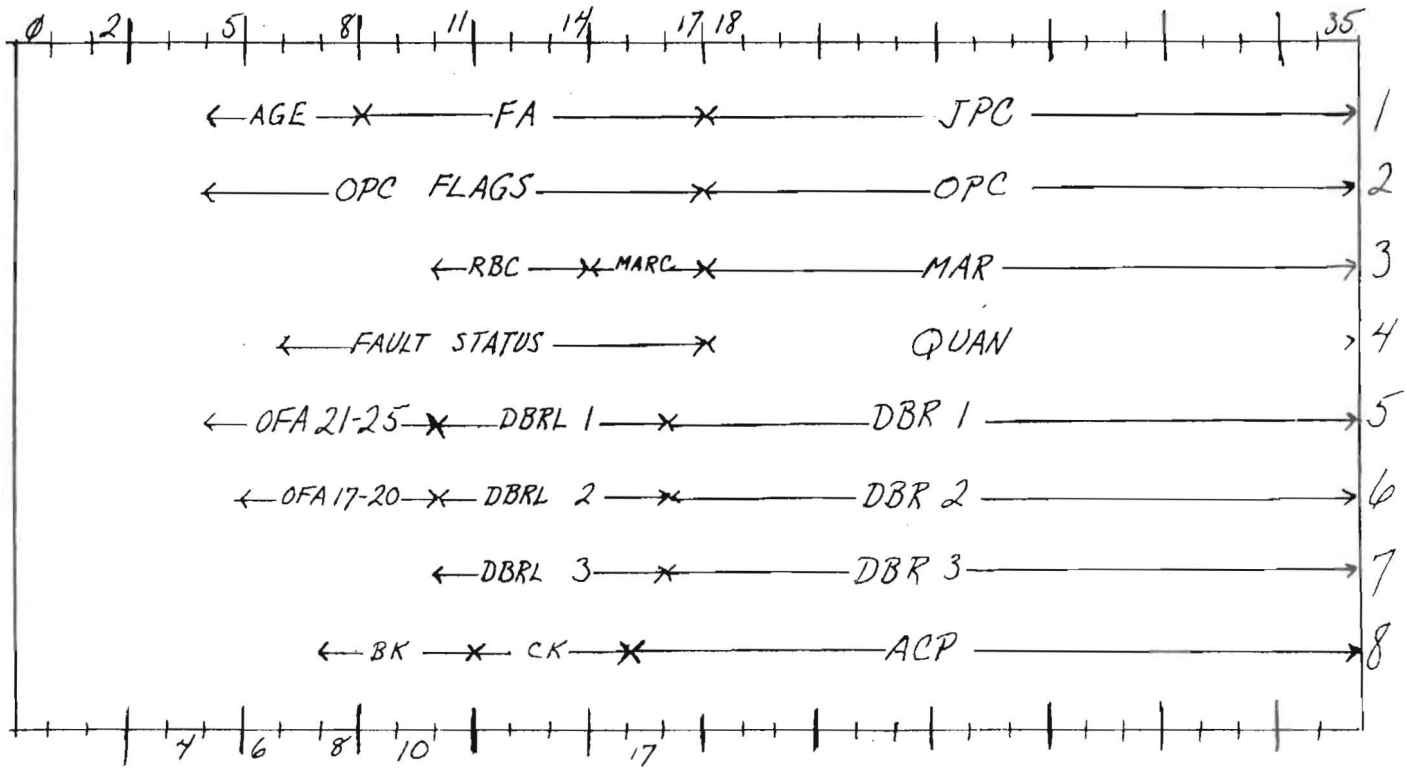
The paging box contains a four-bit program loaded register. Whenever a reference is made to a page word for refilling an AR, bits 5-8 of the page word in core are updated to the current age. This is a method of enabling the executive to differentiate between recently referenced pages versus those that have fallen out of the working set.

3.0 LOAD PAGE MEMORY



An instruction (OP code 12Ø,ØØØ,,) has been added to the PDP-1Ø. This instruction transfers eight words in a block pointed to by the effective address (absolute) to or from the paging device. Load Page Memory (LPM 1Ø2,ØØØ,,) transfers from memory to the paging device, and Store Page Memory (SPM 1Ø2,Ø4Ø,,) writes back in memory the same eight words of state information.

3.1 STATE BLOCK



WD1

5-8 - Age - quantity stored in Age field (5-8, 23-26) of page word when referenced to refill AR.

9-17 - FAULT ADDRESS - virtual address referenced at time of page fault. Bit 9 is a "one" if reference was USER address, 10-17 correspond to MA 18-25.

WD2

5-17 - PC Flags - saved at the beginning of every instruction (except when Priority Interrupt is in progress).

5 - AR OVF (bit Ø of PC word)

6 - AR CRYØ (bit 1)

7 - AR CRY1 (2)

8 - AR FP OVF (3)