EK-DZV11-TM-001

DZV11 asynchronous multiplexer technical manual

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CONTENTS

CONTENTS (Cont)

CONTENTS (Cont)

FIGURES

FIGURES (Cont)

FIGURES (Cont)

TABLES

TABLES (Cont)

CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The DZV11, shown in Figure 1-1, is an asynchronous multiplexer that provides an interface between an LSI-11 processor and four asynchronous serial data communication channels. It can be used with the LSI-11 processor in a variety of applications that include data concentration, real-time processing, and cluster controlling. The DZV11 provides an EIA RS232C interface and enough data set control to permit dial-up (auto-answer) operation with modems capable of full-duplex operation,* such as the Bell models 103, 113, 212, or equivalent. Remote operation over private lines for full-duplex point-to-point or full-duplex multipoint as a control (master) station is also possible. Figure 1-2 depicts several of the possible applications for the DZV11 in an LSI-11 system.

The DZV11 has several features that provide flexible control of parameters such as baud rate, character length, number of stop bits for each line, odd or even parity for each line, and transmitter-receiver interrupts. Additional features include limited data set control, zero receiver baud rate, break generation and detection, silo buffering of received data, and line turnaround.

Program compatibility is maintained with the Unibus option DZ11-A. The only compatibility exception is the number of serial channels supported. The DZV11 does not support 20 mA operation.

1.2 PHYSICAL DESCRIPTION

The DZV11 comprises a single quad size module, 21.6 × 26.5 cm (8.51 × 10.44 inches), which is designated as the M7957 module. All input and output leads are available on a Berg header. The DZV11 connects to the LSI-11 QBus by the H9270 mounting panel or equivalent. All QBus input/output signals enter and leave the module via the mounting panel pins.

1.2.1 DZV11 Configurations

The DZV11 can be supplied in two configurations. The DZV11-A, as shown in Figure 1-1, consists of the M7957 module only. Cabling assemblies for connection to terminals and modem channels are not supplied with the DZV11-A, but are available in the DZV11-B. The DZV11-B consists of an M7957 module, BC11U-25 cable assembly, and two accessory test connectors, H329 and H325. This configuration is shown in Figure 1-3.

*The DZV11 data set control does not support half-duplex operations or the secondary transmit and receive operations available with some modems such as the Bell 202, etc.

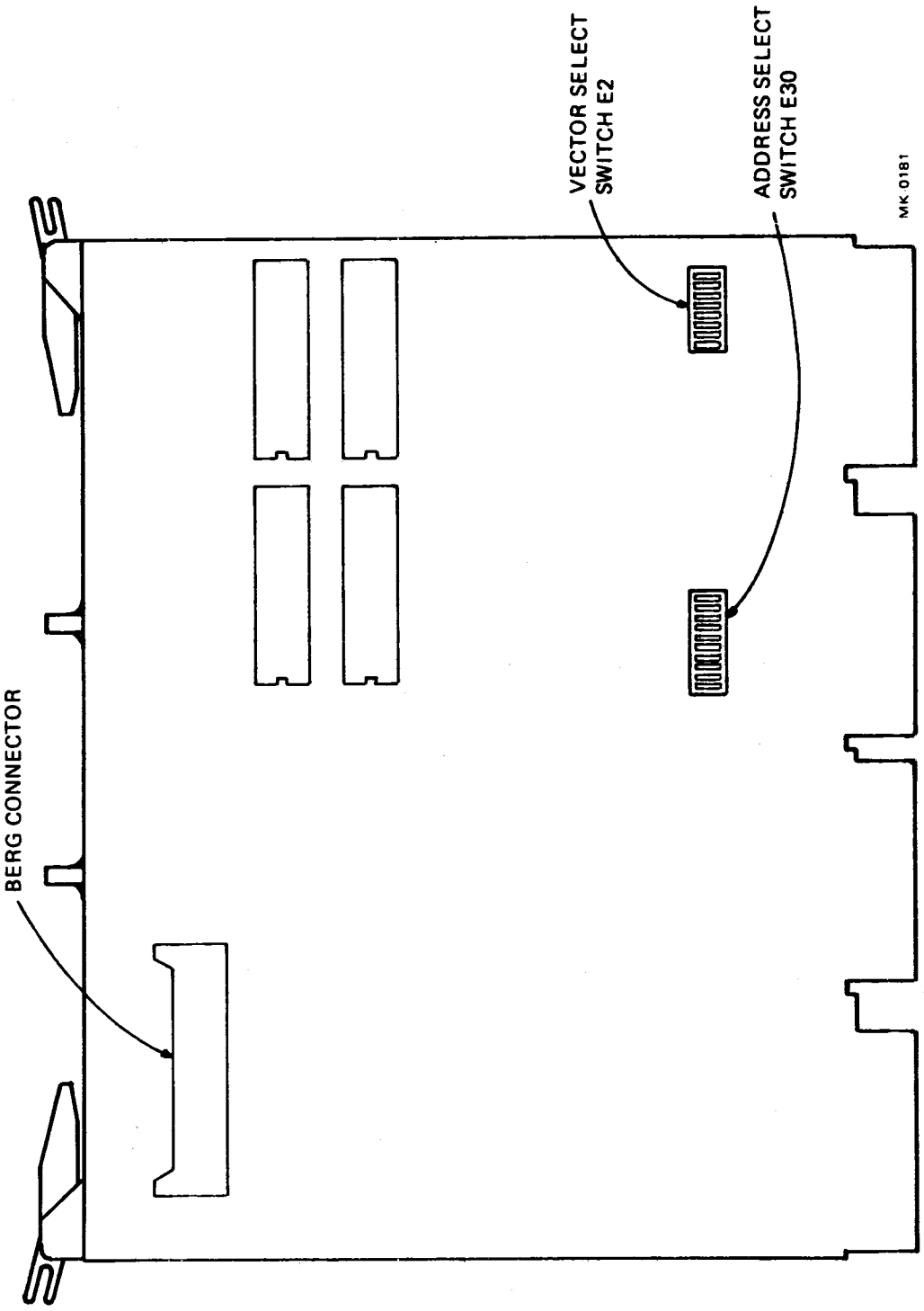


Figure 1-1 DZV11-A (M7957 Module)

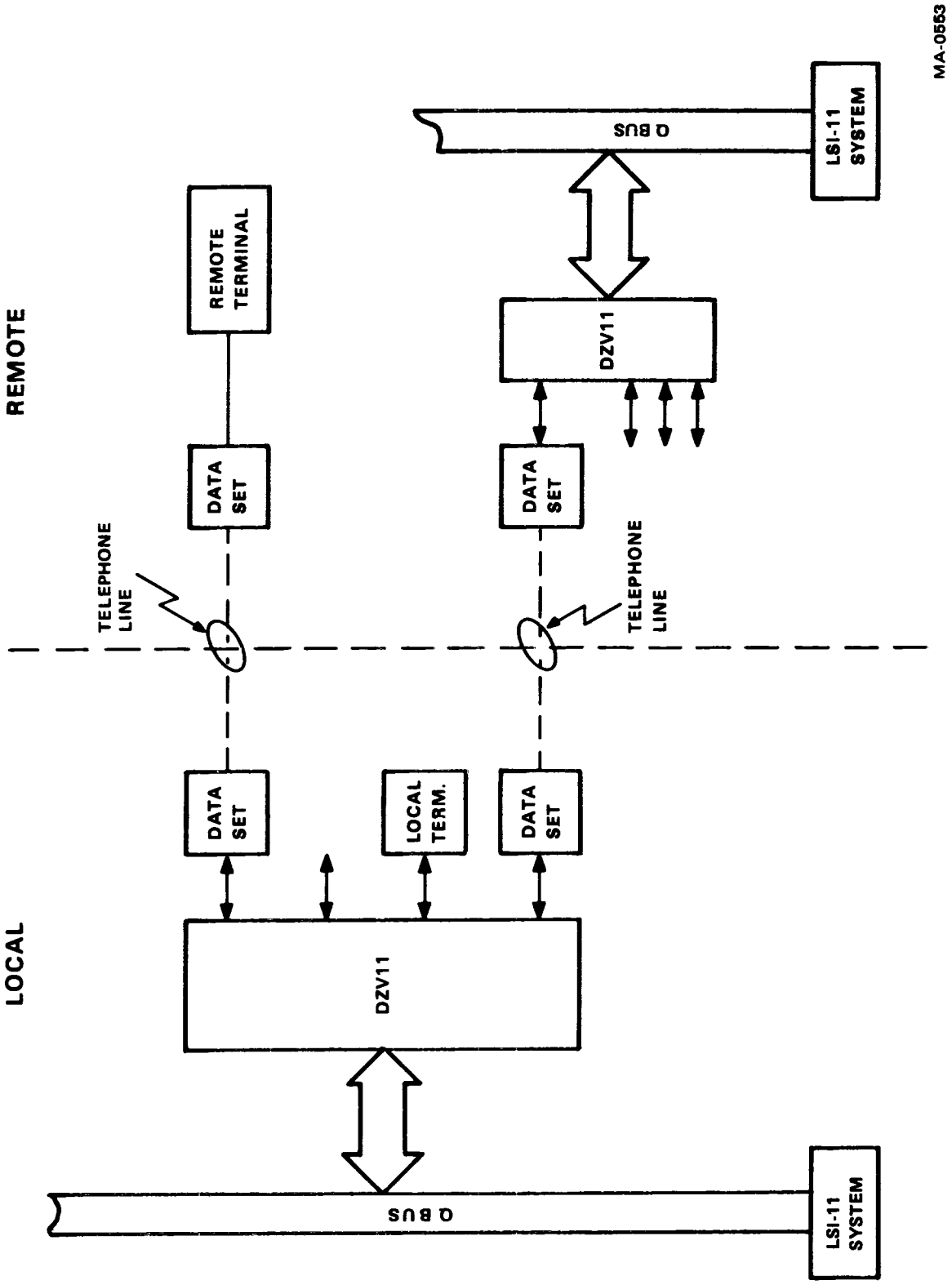


Figure 1-2 DZV11 System Applications

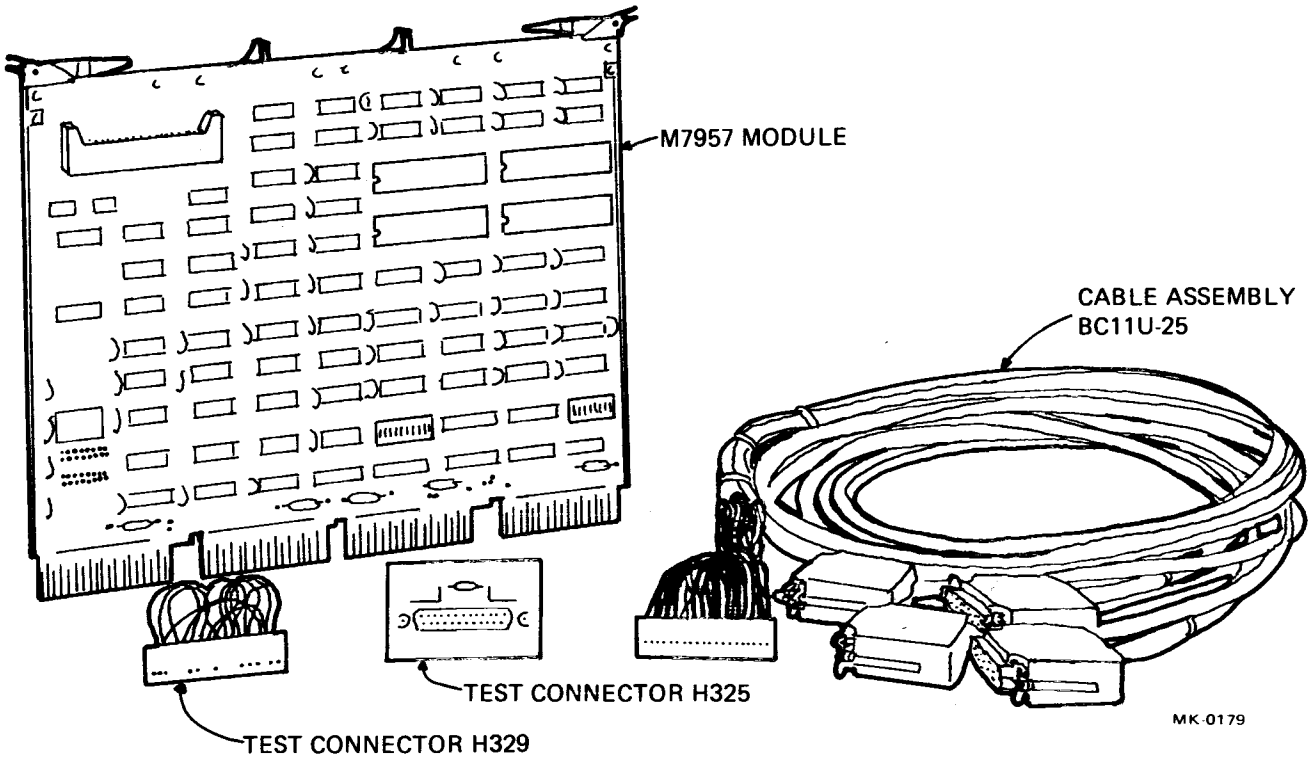


Figure 1-3 DZV11-B (M7957 Module, H325 and H329 Connectors and Cable Assembly BC11U-25)

1.2.2 BC11U Interface Cable

The interfacing cable for terminal and modem connections to the DZV11-B is provided by the BC11U cable assembly (Figure 1-3). It consists of four separate cables, 762 cm (25) in length, each terminated by a separate EIA-type connector housing and a common Berg housing. Each cable within the assembly provides nine input/output leads. The EIA connector pinning conforms to EIA standard RS232C and CCITT* recommendation V.24. The leads supported by the DZV11-B are:

Circuit AA (CCITT 101)	Pin 1	Protective Ground
Circuit AB (CCITT 102)	Pin 7	Signal Ground
Circuit BA (CCITT 103)	Pin 2	Transmitted Data
Circuit BB (CCITT 104)	Pin 3	Received Data
Circuit CD (CCITT 108.2)	Pin 20	Data Terminal Ready
Circuit CE (CCITT 125)	Pin 22	Ring Indicator
Circuit CF (CCITT 109)	Pin 8	Carrier

NOTE

Signal ground and protective ground are connected together.

*CCITT – The Consultive Committee International Telegraph and Telephone is an advisory committee established under the United Nations to recommend worldwide standards.

1.2.3 Test Connectors

Figure 1-4 shows the two accessory test connectors, H329 and H325, that are provided with each DZV11-B. The H325 plugs into an EIA connector on the BC11U to loopback data and modem signals onto a single line. The H329 plugs into the M7957 module socket housing and provides staggered loopback of the data and modem lines. The loopback connections are shown in Figure 1-5.

1.3 SPECIFICATIONS

Environmental, electrical, and performance specifications for the DZV11 are discussed in the following paragraphs.

1.3.1 Environmental

The DZV11 operates in an environment from 5° to 50° C (41° to 122° F) and in a relative humidity of 10 to 95 percent.

1.3.2 Electrical

Power Consumption	1.15 A @ +5 Vdc
	0.39 A @ +12 Vdc

For each line, the DZV11 provides a voltage level interface whose levels and connections conform to EIA standard RS232C and CCITT recommendation V.24. The leads supported by the DZV11 are listed in Paragraph 1.2.2. Each DZV11 meets the LSI-11 QBus interface specification and represents one unit load as an interface.

1.3.3 Performance

The following paragraphs describe the DZV11 performance capabilities and restrictions.

1.3.3.1 Maximum Configurations – The DZV11 multiplexer is assigned a device address in the floating address space. The floating address space starts at 760010 and extends to 764000. A maximum configuration of DZV11s is not limited by floating address space, but is limited by the rules governing an intermediate size system configuration. Therefore, a maximum of seven DZV11 multiplexers may reside in a 9 × 4 backplane.

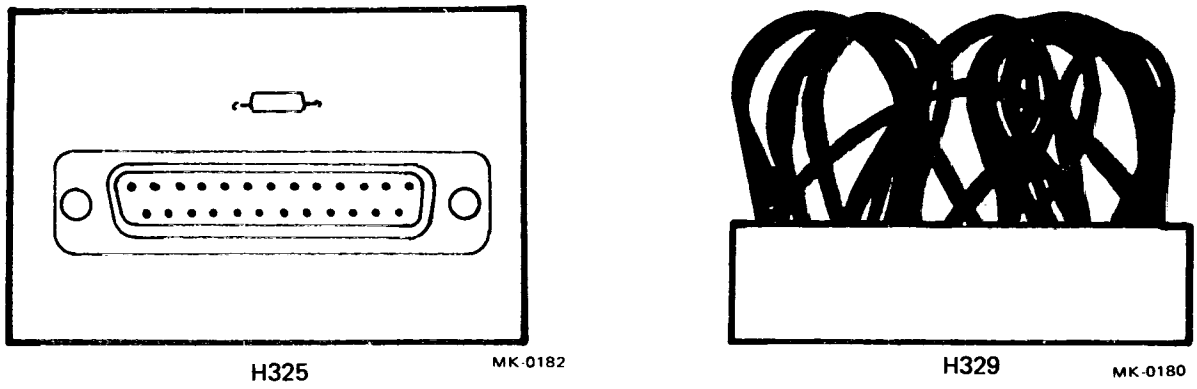


Figure 1-4 Test Connectors H325 and H329

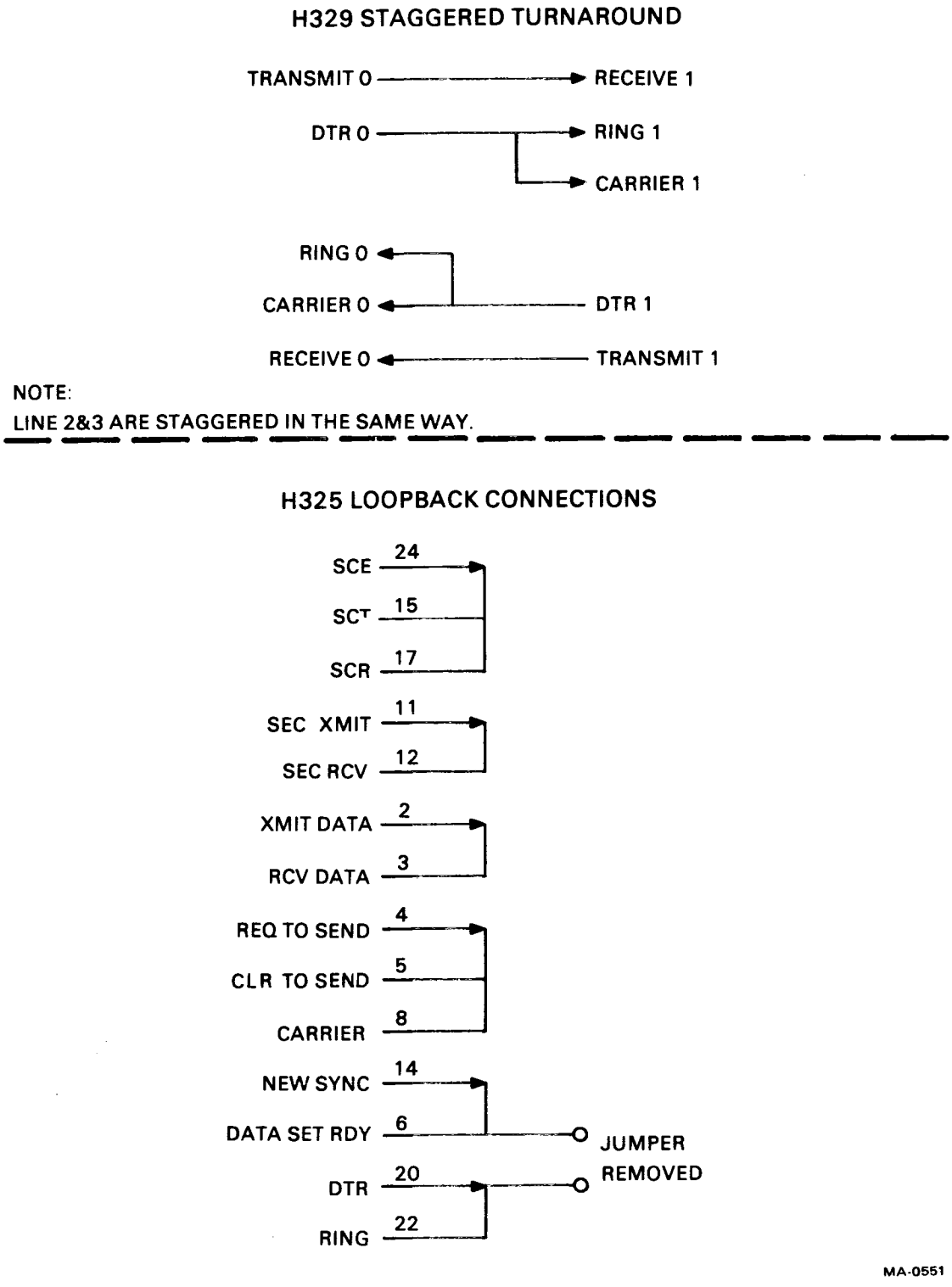


Figure 1-5 Loopback Connections

1.3.3.2 Throughput – Each DZV11 is capable of a throughput rate of 10,970 characters per second. This rate is calculated as follows:

(Bits/second × no. lines × direction) divided by bits/character.
(9600 × 4 × 2) 1/7 equals 10,970 characters/second.

For a character service routine of 100 μs or less, the device throughput rate can be sustained.

1.3.3.3 Receivers – The receivers provide serial- to-parallel conversion of 5-, 6-, 7-, or 8-level code with one start space and at least one stop mark. The character length, number of stop bits, parity generation, and operating speed are programmable parameters for each line. A receiver and transmitter of a corresponding line share the same operating speed with provisions for enabling/disabling of that receive line.

Each receiver is double-buffered and has an allowable input distortion of 43.75 percent on any bit. Also, the accumulated character distortion must not exceed 43.75 percent. Break detection is provided on each receiver.

1.3.3.4 Transmitters – The transmitters provide parallel-to-serial conversion of 5-, 6-, 7- or, 8-level code with or without parity. The parity sense, when selected, can be either odd or even. The stop code can be either 1 or 2 units except when 5-level code is selected. When 5-level code is selected, the stop code can be set to 1 or 1.5 units. The character length, number of stop units, parity generation and sense, and operating speed are programmable parameters for each line. The operating speed for the transmitter is common with the receiver. Breaks are capable of being transmitted on any line. The gross start-stop distortion for a transmitter's TTL output is less than 2.5 percent for an 8-bit character.

1.3.3.5 Baud Rate Generator – The baud rate generator is a MOS/LSI device which provides the DZV11 multiplexer with full programmable capability for operating speed selection. Each line has an independent generator capable of producing 1 of 15 selectable baud rates. Speed tolerance for all rates is less 0.3 percent with a clock duty of 50 percent ± 5 percent. (See below for rates.)

1.3.3.6 Performance Summary – The following summarizes the programmable features offered for each line.

Character length	5-, 6-, 7-, or 8-level code
Number of stop bits	1 or 2 for 6-, 7-, or 8-level code 1 or 1.5 for 5-level code
Parity	Odd, even or none
Baud rates	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, and 9600
Breaks	Can be generated and detected on each line.

1.3.4 Interrupts

The following interrupts are available on the DZV11.

Receiver Done Interrupt

The Receiver Done interrupt occurs every time a character appears at the output of the receiver buffer register and the Silo Alarm is disabled. It can be enabled or disabled from the bus.

Silo Alarm Interrupt
The Silo Alarm interrupt occurs after 16 entries have been made into the receive buffer register by the scanner. This interrupt disables the Receiver Done interrupt and is rearmed when the receive buffer register has been read.

Transmit Interrupt
The Transmit interrupt occurs every time the scanner finds a UART buffer empty condition, and the transmitter control register bit is set for that line. It can be enabled or disabled from the bus.

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter contains the procedures for the unpacking, installation, and initial checkout of the DZV11 Asynchronous Multiplexer.

2.2 UNPACKING AND INSPECTION

The DZV11 is packaged in accordance with commercial packaging practices. First, remove all packing material and check the equipment against the shipping list. (Table 2-1 contains a list of supplied items per configuration.) Report damage or shortages to the shipper immediately and notify the DIGITAL representative. Inspect all parts and carefully inspect the module for cracks, loose components, and separations in the etched paths.

Table 2-1 Items Supplied per Configuration

Quantity	Description	A	B
1	M7957 module	X	X
1	BC11U-25 cable assembly		X
1	H329 test connector		X
1	H325 test connector		X
1	Print set (B-TC-DZV11-0-1) DZV11-A and -B Order number MP00462	X	X
1	Software kit ZJ251-RB	X	X
1	*DZV11 User's Guide* (EK-DZV11-UG)	X	X

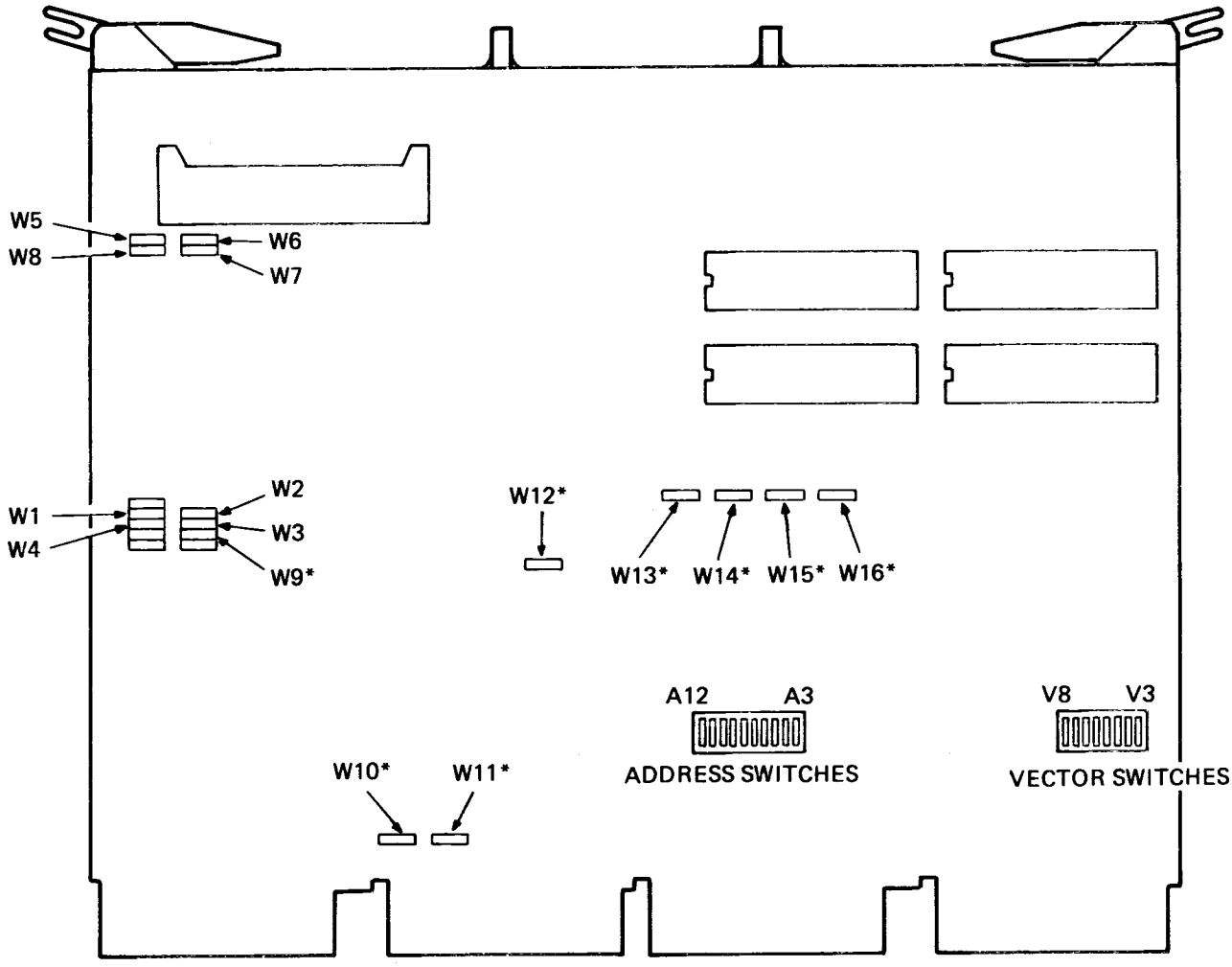
2.3 INSTALLATION PROCEDURE

The following paragraphs describe the installation of the DZV11 option in an LSI-11 system.

2.3.1 Jumper Configuration

There are 16 machine-insertable jumpers on the M7957 module (Figure 2-1).

2.3.1.1 Device Operation – Jumpers W10 and W11 must be installed only when the module is used on an H9270 backplane, or one that applies LSI-11 bus signals to the C and D sections of the module.



*NOTES:

JUMPERS W9, W12, W13, W14, W15, AND W16 ARE REMOVED ONLY FOR MANUFACTURING TESTS. THEY SHOULD NOT BE REMOVED IN THE FIELD.

JUMPERS W10 AND W11 MUST REMAIN INSTALLED WHEN THE MODULE IS USED IN A BACKPLANE THAT SUPPLIES LSI-11 BUS SIGNALS TO THE C AND D CONNECTORS OF THE DZV11 (SUCH AS THE H9270). WHEN THE MODULE IS USED IN A BACKPLANE THAT INTERCONNECTS THE C AND D SECTIONS TO AN ADJACENT MODULE, JUMPERS W10 AND W11 MUST BE REMOVED.

MK-0064

Figure 2-1 M7957 Jumper Locations

2.3.1.2 Modem Control Jumpers – There are eight jumpers used for modem control. The jumpers labeled W1 through W4 connect Data Terminal Ready (DTR) to Request To Send (RTS). This allows the DZV11 to assert both DTR and RTS if using a modem that requires control of RTS. These jumpers must be installed to run the cable and external test diagnostic programs. The remaining four jumpers, W5 through W8, connect the Forced Busy (FB) leads to the RTS leads. With these jumpers installed, the assertion of an RTS lead places an ON or BUSY signal on the corresponding Forced Busy lead. The Forced Busy jumpers (W5 through W8) are normally cut out unless the modem requires them (Table 2-2).

Table 2-2 Jumper Configuration

Jumper	Connection	Line
W1	DTR to RTS	03
W2	DTR to RTS	02
W3	DTR to RTS	01
W4	DTR to RTS	00
W5	RTS to FB	03
W6	RTS to FB	02
W7	RTS to FB	01
W8	RTS to FB	00

2.3.2 Module Installation

To install the M7957 module, perform the following.

1. Refer to Paragraph 4.2 for descriptions of the address assignments. Set the switches at E30 so that the module responds to its assigned address. When a switch is closed (ON), a binary 1 is decoded. When a switch is open (OFF), a binary 0 is decoded. Note that the switch labeled 1 corresponds to address bit 12, 2 corresponds to address bit 11, etc. (Figure 2-2 and Table 2-3).

2. Vector selection is accomplished by the 8-position switch at E2. Switch positions 7 and 8 are not used. Switch position 6 corresponds to vector bit 3, 5 corresponds to vector bit 4, etc. When a switch is closed (ON), a binary 1 is decoded. When a switch is open (OFF), a binary 0 is decoded (Figure 2-3 and Table 2-4).

3. If the module is part of the DZV11-A option, perform step 3. If it is a part of the DZV11-B option, proceed to step 4 for testing.

   a. Insert the module in a quad QBus slot of the backplane.

   CAUTION
   Insert and remove modules slowly and carefully to avoid snagging module components on the card guides and changing switch settings inadvertently.

   b. Run the DZV11 diagnostics, MAINDECs DVDZA and DVDZB, in internal mode to verify operation. Refer to the listing for assistance. Run at least three passes without error.

   c. Proceed to step 8.

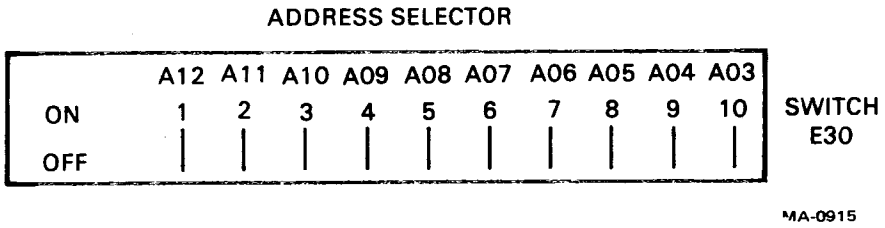


Figure 2-2 M7957 Address Selection

Table 2-3 Address Switch Selection

E30 Switch Address	1 A12	2 A11	3 A10	4 A9	5 A8	6 A7	7 A6	8 A5	9 A4	10 A3
160000	–	–	–	–	–	–	–	–	–	–
160010	–	–	–	–	–	–	–	–	–	X
160020	–	–	–	–	–	–	–	–	X	–
160030	–	–	–	–	–	–	–	–	X	X
160040	–	–	–	–	–	–	–	X	–	–
160050	–	–	–	–	–	–	–	X	–	X
160060	–	–	–	–	–	–	–	X	X	–
160070	–	–	–	–	–	–	–	X	X	X
160100	–	–	–	–	–	–	X	–	–	–
.										
.										
.										
.										
163760	–	–	X	X	X	X	X	X	X	–
163770	–	–	X	X	X	X	X	X	X	X

NOTE: X = ON
– = OFF

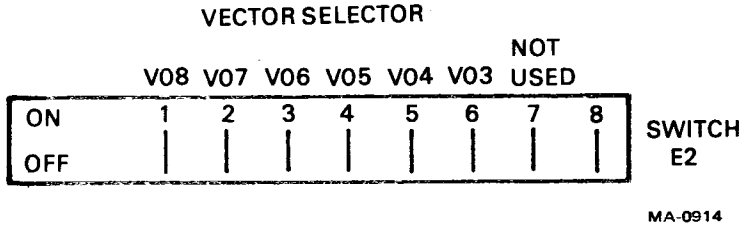


Figure 2-3 M7957 Vector Selection

Table 2-4 Vector Switch Selection

E2 Switch Vector	1 V08	2 V07	3 V06	4 V05	5 V04	6 V03
300	-	X	X	-	-	-
310	-	X	X	-	-	X
320	-	X	X	-	X	-
330	-	X	X	-	X	X
340	-	X	X	X	-	-
350	-	X	X	X	-	X
360	-	X	X	X	X	-
370	-	X	X	X	X	X
400	X	-	-	-	-	-
.						
.						
.						
760	X	X	X	X	X	-
770	X	X	X	X	X	X

NOTE: X = ON
- = OFF

4. Insert the H329 test connector in J1 with the letter side facing up. J1 is the cable connector at the top of the M7957 module.

5. Insert the module in a quad QBus slot of the backplane.

CAUTION

Insert and remove modules slowly and carefully to avoid snagging module components on the card guides and changing switch settings inadvertently.

Run the DZV11 diagnostics, MAINDECs DVDZA and DVDZB, in the staggered mode to verify module operation. Refer to the diagnostic listing for the correct procedure. Run at least three passes without error.

6. Replace the H329 test connector with the Berg end of the BC11U cable assembly. Observe the "This Side Up" wording on the assembly. Refer to D-UA-DZV11-0-0 for installation help.

7. Connect the H325 test connector on the first line and run MAINDEC DVDZC. Select the cable test portion of the diagnostic. Three passes are required without error. Repeat this step for each line.

8. Run DEC/X11 system exerciser to verify the absence of QBus interference with other system devices.

9. The DZV11 is now ready for connection to external equipment. If the connection is to a local terminal through the DZV11-B option, a null modem cable assembly must be used. Use the BC03M or BC03P null modem cables for connection between the BC11U and the terminal. The H312-A null modem unit may also be used in place of the null modem cables. If connection is to a Bell 103 or equivalent modem, install the appropriate line of the BC11U connector into the connector on the modem. A BC05D cable may be required between the BC11U and the modem. Refer to Paragraph 2.3.1.2, Modem Control Jumpers, for selection of jumpers for modem options such as RTS and forced busy. All of the cables mentioned, excluding the BC11U, must be ordered separately as they are not components of a standard DZV11 shipment. When possible, run the diagnostic DVDZC in echo test mode to verify the cable connections and the terminal equipment.

CHAPTER 3
DEVICE REGISTERS

3.1 SCOPE

This chapter provides a description of each DZV11 register, its format, and its bit functions.

3.2 DEVICE REGISTERS

The DZV11 contains six addressable registers. A comprehensive pictorial of these registers' bit assignments is shown in Figure 3-1. Table 3-1 lists the registers and associated DZV11 addresses.

3.2.1 Control and Status Register

The control and status register (CSR) is a byte- and word-addressable register. All bits in the CSR are cleared by an occurrence of BINIT or by setting device Master Clear (CSR 04). The format is shown in Figure 3-1 and the bit assignments are listed in Table 3-2.

3.2.2 Receiver Buffer

The receiver buffer (RBUF) is a 16-bit read-only register that contains the received character at the output of the FIFO buffer. A read of the register causes the character entry to be extracted from the buffer and all other entries to bubble down to the lowest unoccupied location. Only the Valid Data bit (RBUF 15) is cleared by BINIT or by setting device Master Clear (CSR 04). Bits 00–14 are not affected. The bit assignments for the RBUF register are listed in Table 3-3.

Table 3-1 DZV11 Register Address Assignments

Register	Mnemonic	Address	Program Capability
Control and Status Register	CSR	76XXX0	Read/Write
Receiver Buffer	RBUF	76XXX2	Read Only
Line Parameter Register	LPR	76XXX2	Write Only
Transmitter Control Register	TCR	76XXX4	Read/Write
Modem Status Register	MSR	76XXX6	Read Only
Transmit Data Register	TDR	76XXX6	Write Only

XXX = Selected in accordance with floating device address scheme.

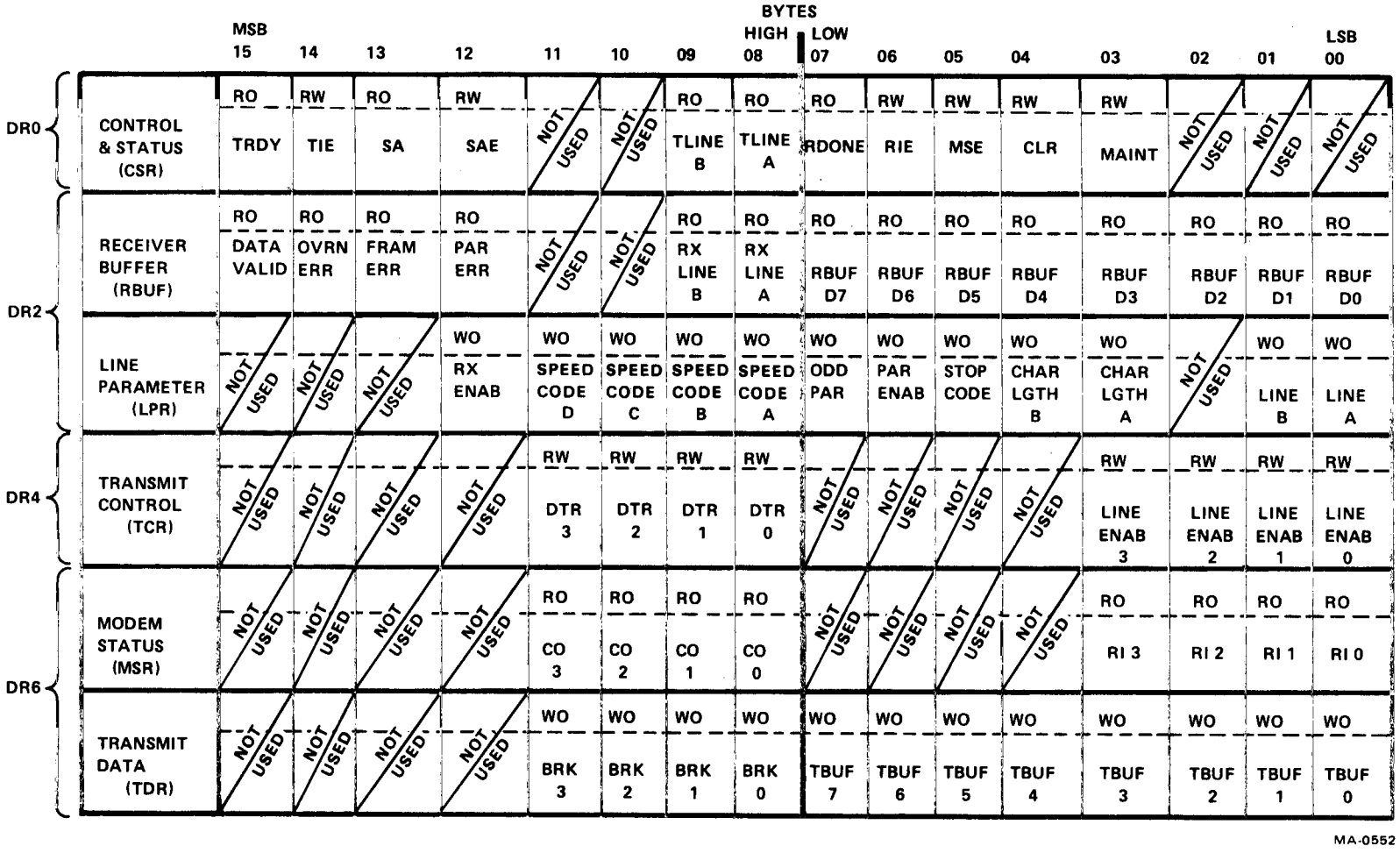


Figure 3-1 Register Bit Assignments

Table 3-2 CSR Bit Assignments

Bit	Title	Function
00–02	Not used	
03	Maintenance	This bit, when set, loops all the transmitter's serial output leads to the corresponding receiver's serial input leads on a TTL basis. While operating in maintenance mode, the EIA received data leads are disabled. Normal operating mode is assumed when this bit is cleared. This bit is read/write.
04	Master Clear	When written to a 1, this bit generates "initialize" within the DZV11. A read-back of the CSR with this bit set indicates initialize in progress within the device. This bit is self-clearing. All registers, silos, and UARTS are cleared with the following exceptions. 1. Only bit 15 of the receiver buffer register (Valid Data) is cleared; the remaining bits 00–14 are not. 2. The high byte of the transmitter control register is not cleared by Master Clear. 3. The modem status register is not cleared by Master Clear.
05	Master Scan Enable	This read/write bit must be set to permit the receiver and transmitter control sections to begin scanning. When cleared, Transmitter Ready (CSR 15) is inhibited from setting and the received character buffers (silos) are cleared.
06	Receiver Interrupt Enable	This bit, when set, permits setting CSR 07 or CSR 13 to generate a receiver interrupt request. This bit is read/ write.
07	Receiver Done	This is a read-only bit that sets when a character appears at the output of the first-in/first out (FIFO) buffer. To operate in interrupt per character mode, CSR 06 must be set and CSR 12 must be cleared. With CSR 06 and CSR 12 cleared, character flag mode is indicated. Receiver Done clears when the receiver buffer register (RBUF) is read or when Master Scan Enable (CSR 05) is cleared. If the FIFO buffer contains an additional character, the Receiver Done flag stays cleared a minimum of 1 μs before presenting that character.
08–09	Transmitter Line Number	These read-only bits indicate the line number whose transmit buffer requires servicing. These bits are valid only when Transmitter Ready (CSR 15) is set and are cleared when Master Scan Enable is cleared. Bit 08 is the least significant bit.
10–11	Not used	

Table 3-2 CSR Bit Assignments (Cont)

Bit	Title	Function
12	Silo Enable Alarm	This is a read/write bit. When set, it enables the Silo Alarm counter to keep count of the number of characters stored in the FIFO buffer. The counter is cleared when the Silo Alarm Enable bit is cleared. Conditioning of this bit must occur prior to any character reception.
13	Silo Alarm	This is a read-only bit set by the hardware after 16 characters have been entered into the FIFO buffer. Silo Alarm is held cleared when Silo Alarm Enable (CSR 12) is cleared. This bit is reset by a read to the receiver buffer register and does not set until 16 additional characters are entered into the buffer. If Receiver Interrupt Enable (CSR 06) is set, the occurrence of Silo Alarm generates a receiver interrupt request. Reception with CSR 06 cleared, permits flag mode operation of the Silo Alarm bit.
14	Transmitter Interrupt Enable	This bit must be set for Transmitter Ready to generate an interrupt. It is read/write.
15	Transmitter Ready	This bit is read only and is set by the hardware. This bit sets when the transmitter clock stops on a line whose transmit buffer may be loaded with another character and whose associated TCR bit is set. The transmitter line number, specified in CSR 08 and CSR 09, is only valid when Transmitter Ready is set. Transmitter Ready is cleared by any of the following conditions. 1. When Master Scan Enable is cleared 2. When the associated TCR bit is cleared for the line number pointed to in CSR 08 and CSR 09 3. At the conclusion of the load instruction of the transmit data register (low byte only) If additional transmit lines require service, Transmitter Ready reappears within 1.4 μs from the completion of the transmit data register load instruction. The occurrence of Transmitter Ready with Transmitter Interrupt Enable set, generates a transmitter interrupt request.

Table 3-3 RBUF Bit Assignments

Bit	Title	Function
00–07	Received Character	These bits contain the received character, right justified. The least significant bit is bit 00. Unused bits are 0. The parity bit is not shown.
08–09	Received Character Line Number	These bits contain the line number upon which the Received Character was received. Bit 08 is the least significant bit.
10–11	Not used	
12	Parity Error	This bit is set if the sense of the parity of the received character does not agree with that designated for that line.
13	Framing Error	This bit is set if the received character did not have a stop bit present at the proper time. This bit is usually interpreted as indicating the reception of a break.
14	Overrun Error	This bit is set if the received character was preceded by a character that was lost due to the inability of the receiver scanner to service the UART receiver holding buffer on that line.
15	Valid Data	This bit, when set, indicates that the data presented in bits 00–14 is valid. This bit permits the use of a character-handling program that takes characters from the FIFO buffer until there are no more available. This is done by reading this register and checking bit 15 until the program obtains a word for which bit 15 is zero.

3.2.3 Line Parameter Register

The line parameter register (LPR) controls the operating parameters associated with each line in the DZV11. The LPR is a word-addressable, write-only register. The line parameters for all lines must be reloaded following an occurrence of either BINIT or device Master Clear. Table 3-4 lists bit assignments.

3.2.4 Transmitter Control Register

The transmitter control register (TCR) is a byte- and word-addressable register. The low byte of the TCR register contains the transmitter control bits which must be set to initiate transmission on a line. Each TCR bit position corresponds to a line number. For example, TCR bit 00 corresponds to line 00, bit 01 to line 01, etc. Setting a TCR bit causes the transmitter scanner clock to stop if the UART for this line has a transmit buffer empty condition. An interrupt is then generated if Transmitter Interrupt Enable is set. The scanner clock restarts when either the transmit data register (TDR) is loaded with a character or the TCR bit is cleared for the line on which the clock has stopped. TCR bits must only be cleared when the scanner is not running (i.e., Transmitter Ready is set or Master Scan Enable is cleared).

Table 3-4 LPR Bit Assignments

Bit	Title	Function
00–01	Parameter Line Number	These bits specify the line number for which the parameter information (bits 3–12) is to apply. Bit 00 is the least significant bit.
02	Not used	Must always be written as a zero when specifying the parameter line number. Writing this bit as a one extends the parameter line number field into nonexistent lines. Parameters for lines 00–03 are not affected.
03–04	Character Length	These bits are set to receive and transmit characters of the length (excluding parity) as shown below. **04 03** 0 0 5 bit 0 1 6 bit 1 0 7 bit 1 1 8 bit
05	Stop Code	This bit sets the stop code length (0 = 1 unit stop, 1 = 2 unit stop or 1.5 unit stop if a 5-level code is employed).
06	Parity Enable	If this bit is set, characters transmitted on the line have an appropriate parity bit affixed, and characters received on the line have their parity checked.
07	Odd Parity	If this bit is set and bit 06 is set, characters of odd parity are generated on the line and incoming characters are expected to have odd parity. If this bit is not set, but bit 06 is set, characters of even parity are generated on the line, and incoming characters are expected to have even parity. If bit 06 is not set, the setting of this bit is immaterial.
08–11	Speed Code	The state of these bits determines the operating speed for the transmitter and receiver of the selected line. **11 10 09 08 Baud Rate** 0 0 0 0 50 0 0 0 1 75 0 0 1 0 110 0 0 1 1 134.5 0 1 0 0 150 0 1 0 1 300 0 1 1 0 600 0 1 1 1 1200 1 0 0 0 1800 1 0 0 0 2000 1 0 1 0 2400

Table 3-4 LPR Bit Assignments (Cont)

Bit	Title	Function				
08–11 (cont)	Speed Code (cont)	**11**	**10**	**09**	**08**	**Baud Rate**
		1	0	1	1	3600
		1	1	0	0	4800
		1	1	0	1	7200
		1	1	1	0	9600
		1	1	1	1	Invalid
12	Receiver Enable	This bit must be set before the UART receiver logic can assemble characters from the serial input line. This bit is cleared following a BINIT or device Master Clear.				
13–15	Not used					

The TCR bits are represented in bits 00–03. These bits are read/write and are cleared by BINIT or device Master Clear. Bits 04–07 are unused and read as zero.

The high byte of the TCR register contains the writable modem control lead, data terminal ready (DTR). Bit designations are as follows.

Bit	Name
08	DTR Line 00
09	DTR Line 01
10	DTR Line 02
11	DTR Line 03
12–15	Unused; read as zero

Assertion of a DTR bit puts an ON condition on the appropriate modem circuit for that line. DTR bits are read/write and are cleared only by BINIT. Jumpers have been provided to allow the RTS circuits to be asserted with DTR assertions.

3.2.5 Modem Status Register

The modem status register (MSR) is a 16-bit read-only register. A read to this register results in the status of the readable modem control leads, Ring and Carrier. The ON condition of a modem control lead is interpreted as a logical one. Bits 04–07 and 12–15 are unused and read as a zero. Remaining bit designations are as follows.

Bit	Name	Bit	Name
00	Ring Line 00	08	Carrier Line 00
01	Ring Line 01	09	Carrier Line 01
02	Ring Line 02	10	Carrier Line 02
03	Ring Line 03	11	Carrier Line 03
04–07	Unused; read as zero.	12–15	Unused; read as zero.

3.2.6 Transmit Data Register

The transmit data register (TDR) is a byte- and word-addressable, write-only register. Characters for transmission are loaded into the low byte. TDR bit 00 is the least significant bit. Loading of a character should occur only when Transmitter Ready (CSR 15) is set. The character that is loaded into this register is directed to the line defined in CSR bits 08 and 09. The high byte of the TDR is designated as the break control register.

Each of the four multiplexer lines has a corresponding break bit for that line. TDR bit 08 represents the break bit for line 00, TDR bit 09 for line 01, etc. TDR bits 12–15 are unused. Setting a break bit forces that line's output to space. This condition remains until cleared by the program. This register is cleared by BINIT or device Master Clear. The break control register can be utilized regardless of the state of the device Maintenance bit (CSR 03).

CHAPTER 4
PROGRAMMING

4.1 SCOPE

This chapter contains information for programming the DZV11 in the most efficient manner. To do so, the programming controls must be fully understood. The following paragraphs discuss the DZV11 from the programming point of view and describe recommended programming methods.

4.2 DEVICE ADDRESS ASSIGNMENTS

The device address assigned to the DZV11 resides in the floating address space of the LSI-11. This address space ranges from 160010_8 to 163776_8. Each DZV11 requires increments of 10_8 address locations and the first option should be configured with an address of 160010_8. The initial configured address assumes that the system consists of only DZV11s in the floating address field. If the DUV11 option is also configured in the floating address field, assign the DZV11 an address that establishes a gap of 10_8 address locations between the last DUV11 and the first DZV11. For example: If the system consists of one DUV11 located at 160010_8, the DZV11 should be configured with an address of 160030_8.

4.3 INTERRUPT VECTOR ADDRESS ASSIGNMENTS

The DZV11 device vector address is selected from the floating vector space. This space ranges from address 300_8 to address 776_8. Each DZV11 requires increments of 10_8 address locations for its two contiguous interrupt vectors. If the DZV11 is the only option in the floating vector area, configure it for a vector of 300_8. If there are options other than the DZV11 residing in the floating vector area, other configuration rules must be applied. When configuring the device vector, only the first vector address must be considered. The first vector, or base vector, must start on a zero boundary.

A zero boundary is one that has the three least significant bits equal to zero. The second vector is controlled by the first vector and data bit 02. Data bit 02 is generated by the M7957 hardware.

Any option ahead of DZV11 in the floating vector space that is not in the configuration should not occupy any vector space gap. For example, if only DZV11 is in the system, the vector for DZV11 should be 300. The simplest case is as follows.

Option	Address	Vector	Comment
GAP	160010	–	No QBus-compatible DJ11
GAP	160020	–	No QBus-compatible DH11
GAP	160030	–	No QBus-compatible DQ11
GAP	160040	–	No DUV11
GAP	160050	–	No QBus-compatible DUP11
GAP	160060	–	No QBus-compatible LK11
GAP	160070	–	No QBus-compatible DMC11
DZV11	160100	300	
GAP	160110	–	No more DZV11s

Each DZV11 requires two interrupt vectors, one for the transmitter section and one for the receiver section. If simultaneous interrupt requests are generated from each section, the receiver section would have priority in placing its vector onto the LSI bus. A receiver interrupt to address XX0 is generated from having either a Receiver Done (CSR 07) or Silo Alarm (CSR 13) occurrence. A transmitter interrupt to address XX4 is generated by Transmitter Ready (CSR 15). Additional prerequisites for generating interrupts are that the individual interrupt enable bits (CSR 06 and CSR 14) be set. The recommended method of clearing interrupt enable bits is first to raise the processor status word to level 4; next, to clear these interrupt enable bits; and then lower the processor status word to zero. Using this method prevents false interrupts from being generated.

4.4 PROGRAMMING FEATURES

The DZV11 has several programming features that allow control of baud rate, character length, stop bits, parity, and interrupts. This paragraph discusses the application of these controls to achieve the desired operating parameters.

4.4.1 Baud Rate

Selection of the desired transmission and reception speed is controlled by the conditions of bits 08–11 of the LPR. Table 4-1 depicts the required bit configuration for each operating speed. The baud rate for each line is the same for both the transmitter and receiver. The receiver clock is turned on and off by setting and clearing bit 12 in the LPR for the selected line.

Table 4-1 Baud Rate Selection Chart

Bits				
11	**10**	**09**	**08**	**Baud Rate**
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	Not used

4.4.2 Character Length

The selection of one of the four available character lengths is controlled by bits 03 and 04 of the LPR. The bit conditions for bits 04 and 03, respectively, are as follows: 00 (5-level), 01 (6-level), 10 (7-level), and 11 (8-level). For character lengths of 5, 6, and 7, the high-order bits of the received character are forced to zero.

4.4.3 Stop Bits

The length of the stop bits in a serial character string is determined by bit 05 of the LPR. If bit 05 is a zero, the stop length is one unit; bit 05 set to a one selects a 2-unit stop unless the 5-level character length (bits 03 and 04 at zero) is selected, in which case the stop bit length is 1.5 units.

4.4.4 Parity

The parity option is selected by bit 06 of the LPR. Parity is enabled on transmission and reception by setting bit 06 to a one. Bit 07 of the LPR allows selection of even or odd parity, and bit 06 must be set for bit 07 to be significant. The parity bit is generated and checked by hardware and does not appear in the RBUF or TBUF. The parity error (bit 12, RBUF) flag is set when the received character has a parity error.

4.4.5 Interrupts

The Receiver Interrupt Enable (RIE) and Silo Alarm Enable (SAE) bits in the CSR control the circumstances upon which the DZV11 receiver interrupts the LSI-11 processor.

If RIE and SAE are both clear, the DZV11 never interrupts the LSI-11 processor. In this case, the program must periodically check for the availability of data in the silo and empty the silo when data is present. If the program operates off a clock, it should check for characters in the silo at least as often as the time it takes for the silo to fill, allowing a safety factor to cover processor response delays and time to empty the silo. The Receiver Done (RDONE) bit in the CSR sets when a character is available in the silo. The program can periodically check this bit with a TSTB or BIT instruction. When RDONE is set, the program should empty the silo.

If RIE is set and SAE is clear, the DZV11 interrupts the LSI-11 processor to the DZV11 receiver vector address when RDONE is set, indicating the presence of a character at the bottom of the silo. The interrupt service routine can obtain the character by performing a MOV instruction from the RBUF. If the program then dismisses the interrupt, the DZV11 interrupts when another character is available (which may be immediately if additional characters were placed in the silo while the interrupt was being serviced). Alternatively, the interrupt service routine may respond to the interrupt by emptying the silo before dismissing the interrupt.

If RIE and SAE are both set, the DZV11 interrupts the LSI-11 processor to the DZV11 receiver vector when the Silo Alarm (SA) bit in the CSR is set. The SA bit is set when 16 characters have been placed in the silo since the last time the program has accessed the RBUF. Accessing the RBUF clears the SA bit and the associated counter. The program should follow the procedure described in Paragraph 4.4.6 to empty the silo completely in response to an Silo Alarm interrupt. This ensures that any characters placed in the silo while it is being emptied are processed by the program.

NOTE

If the program processes only 16 entries in response to each Silo Alarm interrupt, characters coming in while interrupts are being processed build up without being counted by the Silo Alarm circuit and the silo may eventually overflow without the alarm being issued.

If the Silo Alarm interrupt is used, the program will not be interrupted if fewer than 16 characters are received. In order to respond to short messages during periods of moderate activity, the LSI-11 program should periodically empty the silo. The scanning period depends on the required responsiveness to received characters. While the program is emptying the silo, it should ensure that DZV11 receiver interrupts are inhibited. This should be done by raising the LSI-11 processor priority. The Silo Alarm interrupt feature can significantly reduce the LSI-11 processor overhead required by the DZV11 receiver by eliminating the need to enter and exit an interrupt service routine each time a character is received.

The Transmitter Interrupt Enable (TIE) bit controls transmitter interrupts to the LSI-11 processor. If enabled, the DZV11 interrupts the LSI-11 processor at the DZV11 transmitter interrupt vector when the Transmitter Ready (TRDY) bit in the CSR is set, indicating that the DZV11 is ready to accept a character to be transmitted.

4.4.6 Emptying the Silo

The program can empty the silo by repeatedly performing MOV instructions from the RBUF to temporary storage. Each MOV instruction copies the bottom character in the silo so it is not lost and clears out the bottom of the silo, allowing the next character to move down for access by a subsequent MOV instruction. The program can determine when it has emptied the silo by testing the Data Valid bit in each word moved out of the RBUF. A zero value indicates that the silo has been emptied. The test can be performed conveniently by branching on the condition code following each MOV instruction. The TST or BIT instruction must not access the RBUF because these instructions cause the next entry in the silo to move down without saving the current bottom character. Furthermore, following a MOV from the RBUF, the next character in the silo is not available for at least 1 μs. Therefore, on fast CPUs, the program must use sufficient instructions or NOPs to ensure that successive MOVs from the RBUF are separated by a minimum of 1 μs. This prevents a false indication of an empty silo.

4.4.7 Transmitting a Character

The program controls the DZV11 transmitter through four registers on the QBus: the control and status register (CSR), the line parameter register (LPR), the transmit control register (TCR), and the transmit data register (TDR).

Following DZV11 initialization, the program must use the LPR to specify the speed and character format for each line to be used and must set the Master Scan Enable (MSE) bit in the CSR. The program should set the TIE bit in the CSR if it wants the DZV11 transmitter to operate on a program interrupt basis.

The TCR is used to enable and disable transmission on each line. One bit in this register is associated with each line. The program can set and clear bits by using MOV, MOVB, BIS, BISB, BIC, and BICB instructions. (If word instructions are used, the Line Enable bits and the DTR bits are simultaneously accessed.)

The DZV11 transmitter is controlled by a scanner which is constantly looking for an enabled line (Line Enable bit set) which has an empty UART transmitter buffer. When the scanner finds such a line, it loads the number of the line into the 2-bit transmit line number (TLINE) field of the CSR and sets the TRDY bit, interrupting the LSI-11 processor if the TIE bit is set. The program can clear the TRDY bit by moving a character for the indicated line into the TBUF or by clearing the line enable bit. Clearing the TRDY bit frees the scanner to resume its search for lines needing service.

To initiate transmission on an idle line, the program should set the TCR bit for that line and wait for the scanner to request service on the line, as indicated by the scanner loading the number of the line into TLINE and setting TRDY. The program should then load the character to be transmitted into the TBUF by using a MOVB instruction. If interrupts are to be used, a convenient way of starting up a line is to set the TCR bit in the main program and let the normal transmitter interrupt routine load the character into the TBUF.

NOTE

The scanner may find a different line needing service before it finds the line being started up. This occurs if other lines request service before the scanner can find the line being started. The program must always check the TLINE field of the CSR when responding to TRDY to ensure that it loads characters for the correct line. Assuming the program services lines as requested by the scanner, the scanner eventually finds the line being started. If several lines require service, the scanner requests service in priority order as determined by line number. Line 3 has the highest priority and line 0 the lowest.

To continue transmission on a line, the program should load the next character to be transmitted into the TBUF each time the scanner requests service for the line as indicated by TLINE and TRDY.

To terminate transmission on a line, the program loads the last character normally and waits for the scanner to request an additional character for the line. The program clears the Line Enable bit at this time instead of loading the TBUF.

The normal rest condition of the transmitted data lead for any line is the one state. The Break (BRK) bits are used to apply a continuous zero signal to the line. One bit in the TDR is associated with each line. The line remains in this condition as long as the bit remains set. The program should use a MOVB instruction to access the BRK bits. If the program continues to load characters for a line after setting the BRK bit, transmitter operation appears normal to the program despite the fact that no characters can be transmitted while the line is in the continuous zero sending state. The program may use this facility for sending precisely timed zero signals by setting the BRK bit and using transmit ready interrupts as a timer.

It should be remembered that each line in the DZV11 is double buffered. The program must not set the BRK bit too soon or the two data characters preceding the break may not be transmitted. The program must also ensure that the line returns to the one state at the end of the zero sending period before transmitting any additional data characters. The following procedure accomplishes this. When the scanner requests service the first time after the program has loaded the last data character, the program should load an all-zero character. When the scanner requests service the second time, the program should set the BRK bit for the line. At the end of the zero sending period, the program should load an all-zero character to be transmitted. When the scanner requests service, indicating this character has begun transmission, the program should clear the BRK bit and load the next data character.

4.4.8 Data Set Control

The program may sense the state of the Carrier and Ring Indicator signals for each data set and may control the state of the Data Terminal Ready signal to each data set. The program uses two registers to access the DZV11 data set control logic. There are no hardware interlocks between the data set control logic and the receiver and transmitter logic. Any required coordination should be done under program control.

The Data Terminal Ready (DTR) bits in the TCR are read/write bits. Setting or clearing a bit in this register turns the appropriate DTR signal on or off. The program may access this register with word or byte instructions. (If word instructions are used, the DTR and Line Enable bits are simultaneously accessed.) The DTR bits are cleared by the INIT signal on the QBus but is not cleared if the program clears the DZV11 by setting the CLR bit of the CSR.

The Carrier (CO) and Ring (RI) bits in the MSR are read-only bits. The program can determine the current state of the Carrier signal for a line by examining the appropriate bit in the MSR. It can determine the current state of the Ring signal by examining the appropriate bit of the ring register. The program can examine these registers separately by using MOVB or BITB instructions or can examine them as a single 16-bit register by using MOV or BIT instructions. The DZV11 data set control logic does not interrupt the LSI-11 processor when a Carrier or Ring signal changes state. The program should periodically sample these registers to determine the current status. Sampling at a high rate is not necessary.

CHAPTER 5
TECHNICAL DESCRIPTION

5.1 GENERAL

This chapter describes the DZV11 at three levels: interface, circuit function, and circuit operation. Where practical, the illustrations reference the circuit schematic page number and use the signal mnemonics (Figure 5-1). Signal mnemonics in the Field Maintenance Print Set are prefaced by the page number on which they originate. For example, D12 VALID DATA H originates on sheet D12. The print set is helpful, but not essential, for understanding this chapter.

For further information about the LSI chips used on the DZV11, refer to Appendix A.

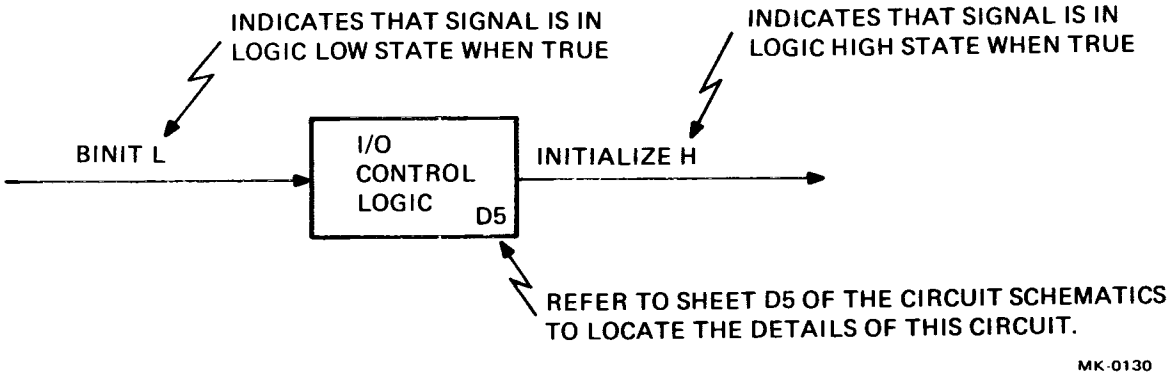


Figure 5-1 Labeling Conventions

5.2 INTERFACE FUNCTIONS

This paragraph illustrates the sequences of signal exchanges that occur among the LSI-11, the DZV11, and data sets. For a detailed description of LSI-11 operation, refer to the *Microcomputer Handbook* (DEC part number EB 07948 53/77). For a discussion of the signals at the circuit level, refer to Pararaph 5.4 of this manual. For information about the specific meaning and function of modem signals, refer to the documentation for the modem with which the DZV11 is to be used.

5.2.1 LSI-11 to DZV11 Interface

Figure 5-2 lists the signals that interface the LSI-11 to the DZV11. Table 5-1 defines these signals. Figures 5-3 through 5-6 indicate their interaction.

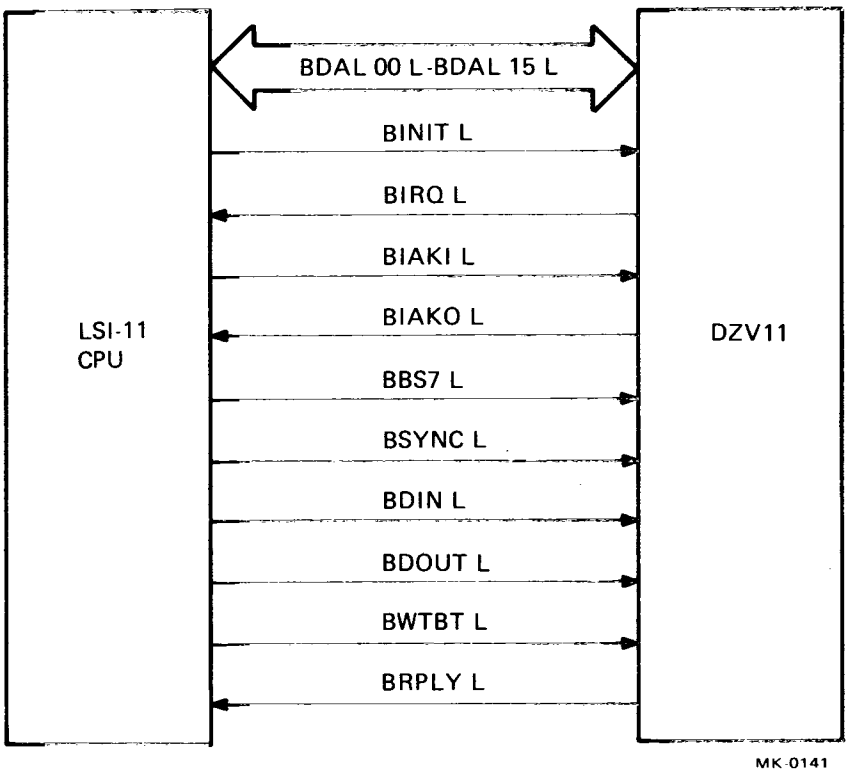


Figure 5-2 LSI-11/DZV11 Interface

Table 5-1 LSI-11/DZV11 Interface Signals

Mnemonic	Description
BINIT L	Initialize – BINIT is asserted by the processor to initialize or clear all devices connected to the I/O bus. The signal is generated in response to a power-up condition.
BIRQ L	Interrupt Request – A device asserts this signal when its interrupt enable and interrupt request flip-flops are set. If the processor's processor status (PS) word bit 7 is 0, the processor responds by acknowledging the request by asserting BDIN L and BIAKO L.
BIAKI L BIAKO L	Interrupt Acknowledge Input and Interrupt Acknowledge Output – This is an interrupt acknowledge signal that is generated by the processor in response to an interrupt request (BIRQ L.) The processor asserts BIAKO L, which is routed to the BIAKI L pin of the first device on the bus. If the device is requesting an interrupt, it inhibits passing BIAKO L. If it is not asserting BIRQ L, the device passes BIAKI L to the next (lower-priority) device via its BIAKO L pin and the lower-priority device's BIAKI L pin.
BBS7 L	Bank 7 Select – The CPU asserts BBS7 L when an address in the upper 4K bank (address in the 28K–32K range) is placed on the bus. BSYNC L is then asserted and BBS7 L remains active for the duration of the addressing portion of the bus cycle.

Table 5-1 LSI-11/DZV11 Interface Signals (Cont)

Mnemonic	Description
BSYNC L	Synchronize – BSYNC L is asserted by the CPU to indicate that it has placed an address on BDAL0-15 L. The transfer is in process until BSYNC L is negated.
BDIN L	Data Input – BDIN L is used for two types of bus operations: 1. When asserted during BSYNC L time, BDIN L implies an input transfer, and requires a response (BRPLY L). BDIN L is asserted when the CPU is ready to accept data from the DZV11. 2. When asserted without BSYNC L, BDIN L indicates that an interrupt operation is occurring.
BDOUT L	Data Output – BDOUT, when asserted, implies that valid data is available on BDAL0-15 L and that an output transfer is taking place. BDOUT L is deskewed with respect to data on the bus. The DZV11 must assert BRPLY L to complete the transfer.
BWTBT L	Write/Byte – BWTBT L is used in two ways to control a bus cycle: 1. It is asserted during the leading edge of BSYNC L to indicate that an output sequence is to follow (DATO or DATOB), rather than an input sequence. 2. It is asserted during BDOUT L, in a DATOB bus cycle, for byte addressing.
BRPLY L	Reply – BRPLY L is asserted in response to BDIN L or BDOUT L and during IAK transaction. It is generated by the DZV11 to indicate that it has placed its data on the BDAL bus or that it has accepted output data from the bus.
BDAL0 L BDAL1 L BDAL2 L BDAL3 L BDAL4 L BDAL5 L BDAL6 L BDAL7 L BDAL8 L BDAL9 L BDAL10 L BDAL11 L BDAL12 L BDAL13 L BDAL14 L BDAL15 L	Data/Address Lines – These lines form a bidirectional bus. First, the CPU places address information on the bus. After the desired device has been addressed, the CPU removes the address. Then data is placed on the bus. For an output transfer, the CPU places the data on the bus. For an input transfer, the DZV11 places the data on the bus.

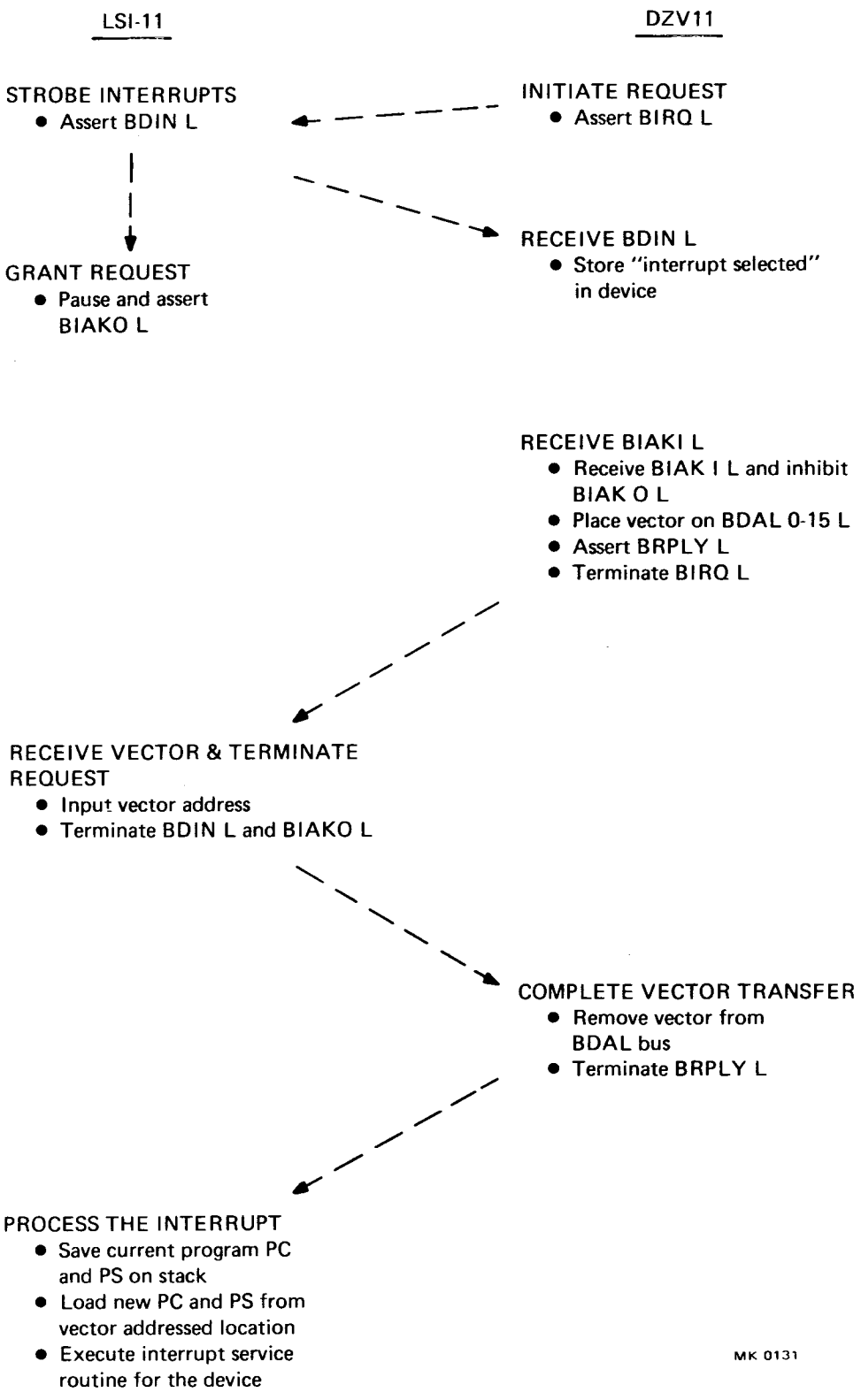


Figure 5-3 Interrupt Request/Acknowledge Sequence

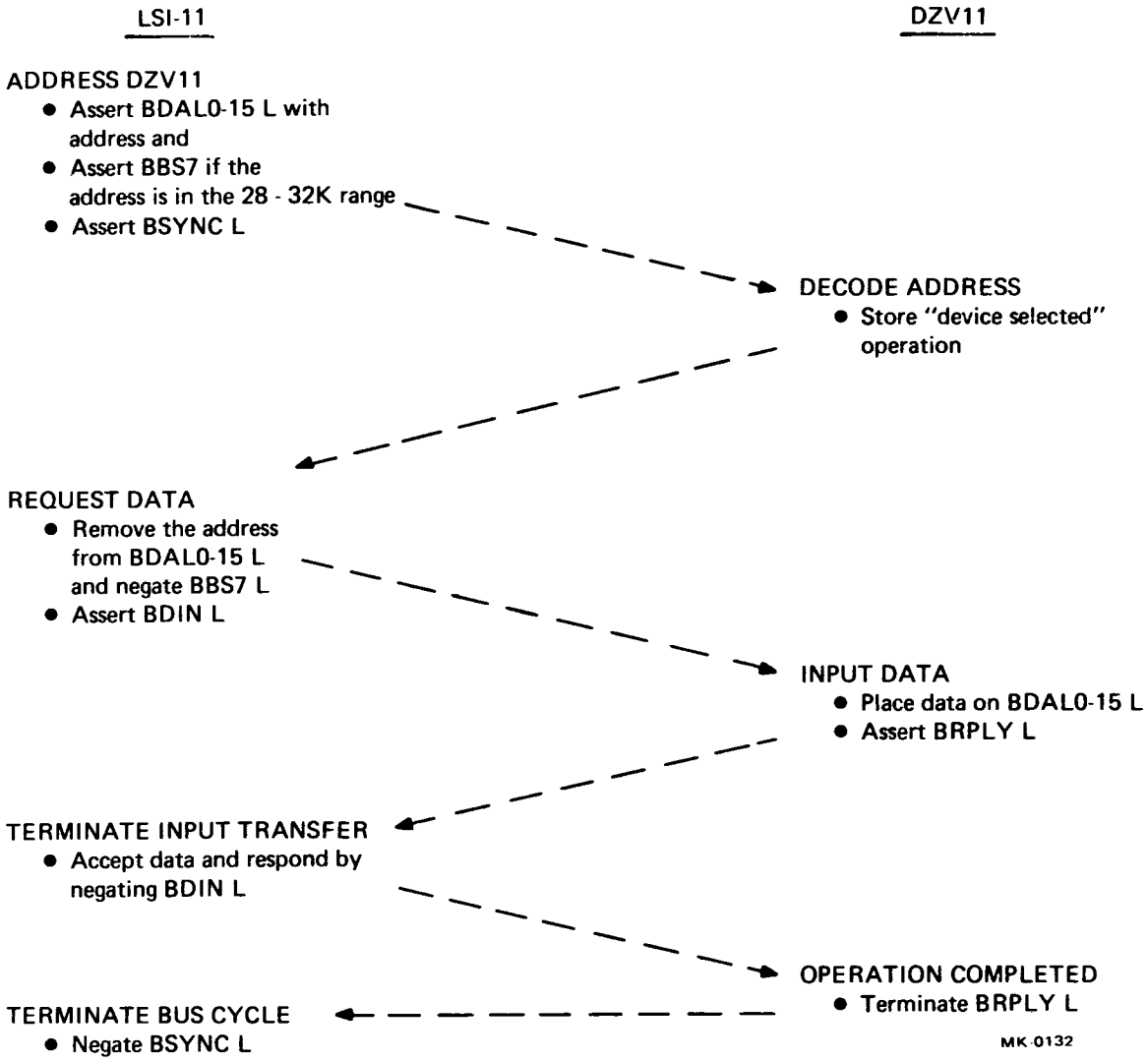


Figure 5-4 DATI Bus Cycle

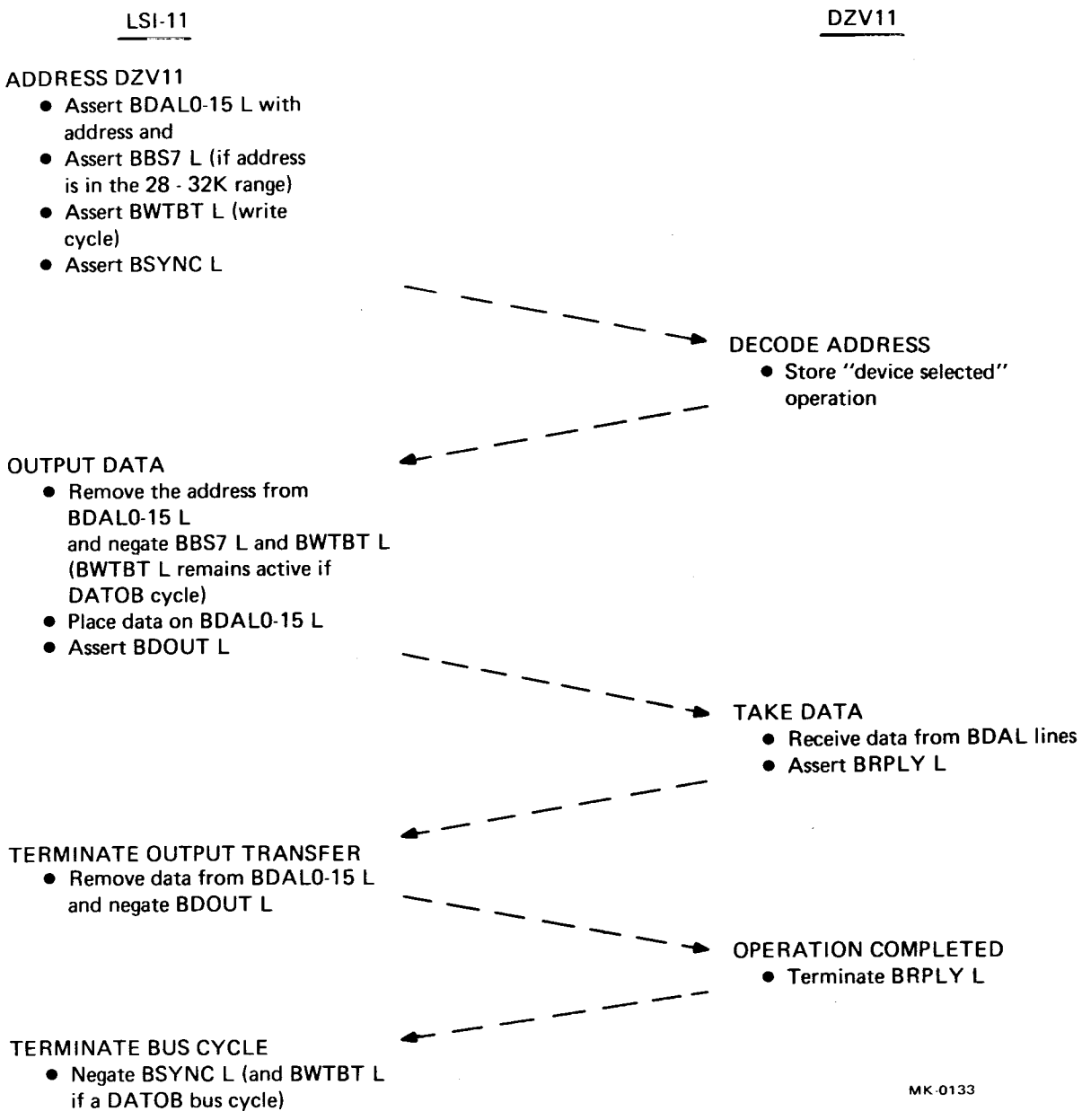


Figure 5-5 DATO or DATOB Bus Cycle

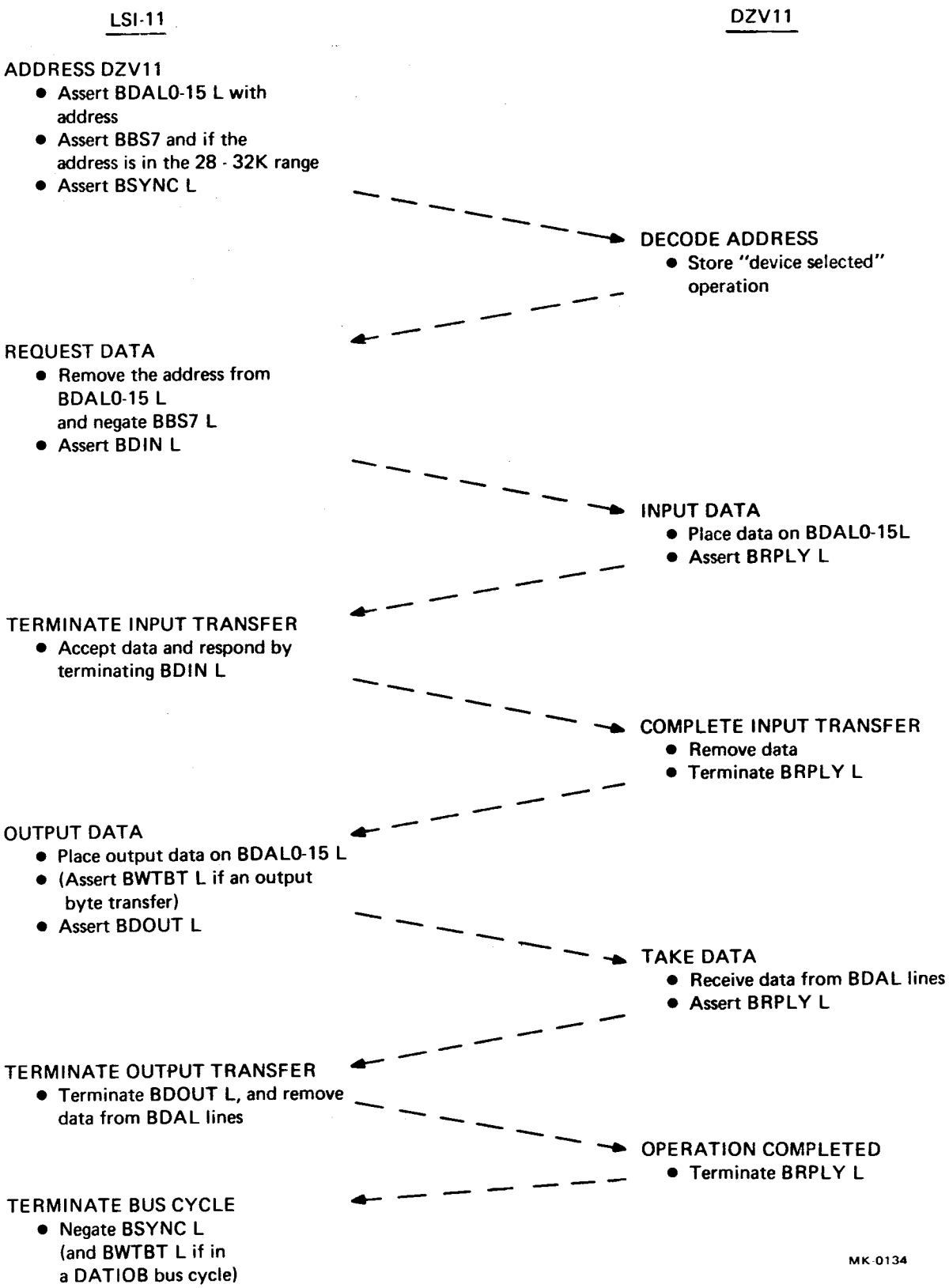


Figure 5-6 DATIO or DATIOB Bus Cycle

Transactions between the LSI-11 and the DZV11 may be program-initiated or interrupt-driven. An interrupt-driven transaction is illustrated in Figure 5-3. An input operation (DATI) is equivalent to a read operation. An output operation (DATO or DATOB) is equivalent to a write operation. A DATI reads a word. A DATO writes a word. A DATOB writes a byte. These operations are described further in Paragraph 5.4.

A DATIO cycle is equivalent to a read-modify-write operation. An addressing operation and an input word transfer are first executed in a manner similar to the DATI cycle; however, BSYNC L remains in the active state after completing the input data transfer. This causes the addressed device or memory to remain selected, and an output data transfer follows without any further addressing. After completing the output data transfer, the device terminates BSYNC L, completing the DATIO cycle. The sequence required for a DATIO cycle is shown in Figure 5-6. Note that the output data transfer portion of the bus cycle can also be a byte transfer. This is a DATIOB cycle. Figure 5-6 illustrates both.

5.2.2 DZV11 to Data Set Interface

When the DZV11 interfaces a local terminal, the only exchanges may be EIA level data. When interfacing a data set, however, the DZV11 controls from one to three signals, and monitors two others.

Table 5-2 defines the modem control signals. Figures 5-7 through 5-9 illustrate typical sequences. The response the DZV11 makes to the Ring and Carrier signals is under program control.

Table 5-2 Modem Control Signals

Signal	Function
Data Terminl Ready	Enables the local modem to be connected with a remote modem. This signal is negated to terminate a call.
Request to Send	Holds the modem in the transmit mode.
Forced Busy	Used with Bell Model 103E and 113B equipment. Signals the modem controller to switch to another channel.
Ring Indicator	Indicates that the local modem is receiving a ringing signal from a remote modem.
Carrier (Received Line Signal Detector)	Indicates that the local modem is receiving a signal from a remote modem, and that the signal meets the suitability criteria of the local modem.

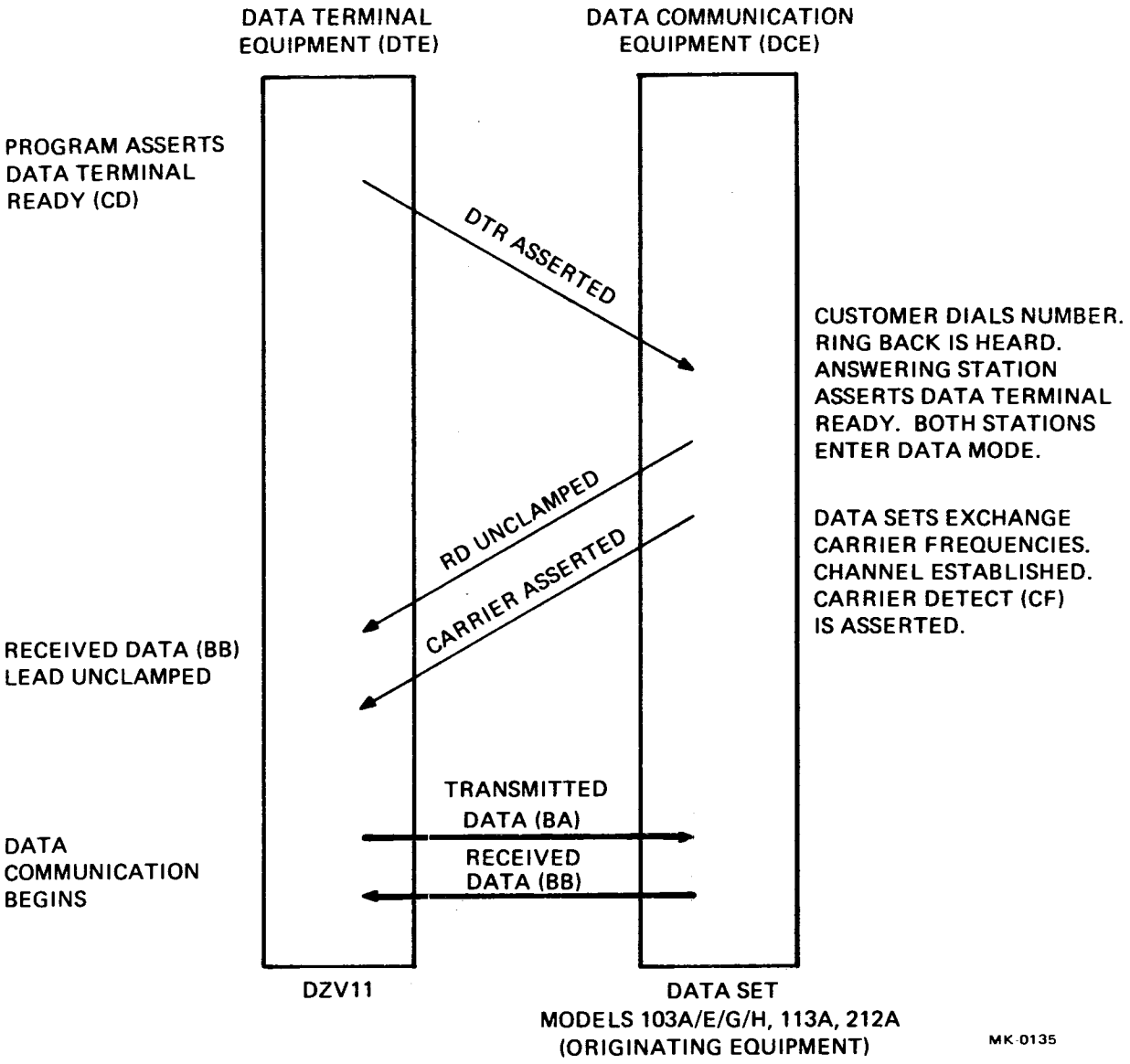
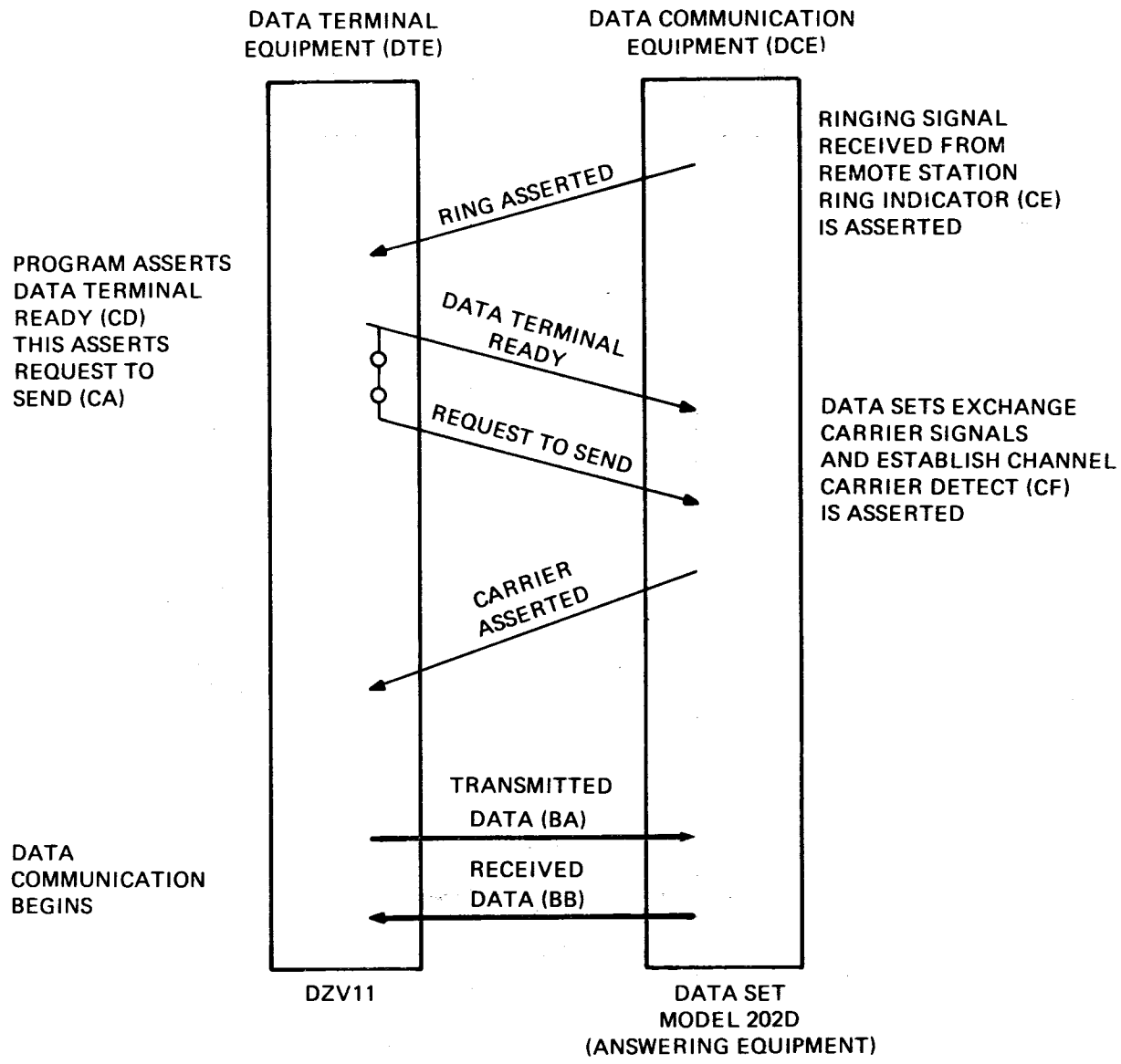


Figure 5-7 Channel Established by Local Modem



NOTE:
EXAMPLE SHOWS MODEM CONFIGURED FOR UNATTENDED ANSWERING AND FULL DUPLEX DATA-PHONE SERVICE. (DATA-PHONE IS A SERVICE MARK OF THE AT & T CO.)

MK-0136

Figure 5-8 Channel Established by Remote Modem

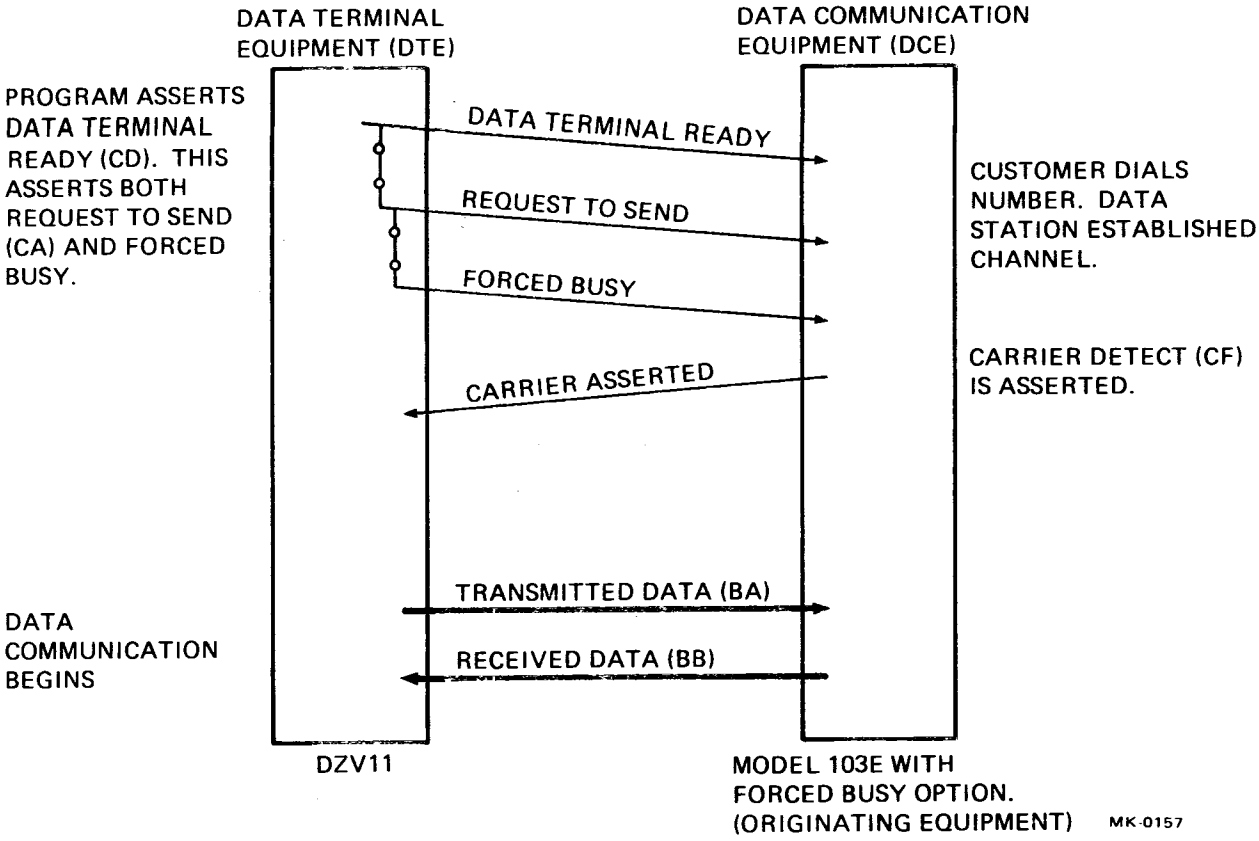


Figure 5-9 Interface with Bell Data Station

5.3 CIRCUIT FUNCTIONS

The major functional areas of the DZV11 circuitry are represented in Figure 5-10. The numbers in the blocks refer to the paragraphs in which the block is discussed.

Data to be transmitted on the communication lines moves from the LSI-11 bus through the bus interface to the TDR in the UARTs. There it is converted from parallel to serial and sent to the EIA transmitters. The transmitters convert the serial data from TTL to EIA levels and send it to the communication line (or data set.)

Data coming in from the communication lines is converted from EIA to TTL by the EIA receivers, then from serial to parallel by the UARTs. The parallel data leaves the UART receiver buffers and is stored in the silo buffer. From there it is transferred via multiplexers to the bus interface. The bus interface places the data on the LSI-11 bus.

The interrupt logic requests interrupt service when a transmitter is empty and when the silo buffer has either 1 or 16 characters of received data, as selected by the program.

The transmitter control determines which of the four possible lines is to be used, and controls the loading of the data.

The receiver control scans the receiver status and controls the loading and unloading of the silo.

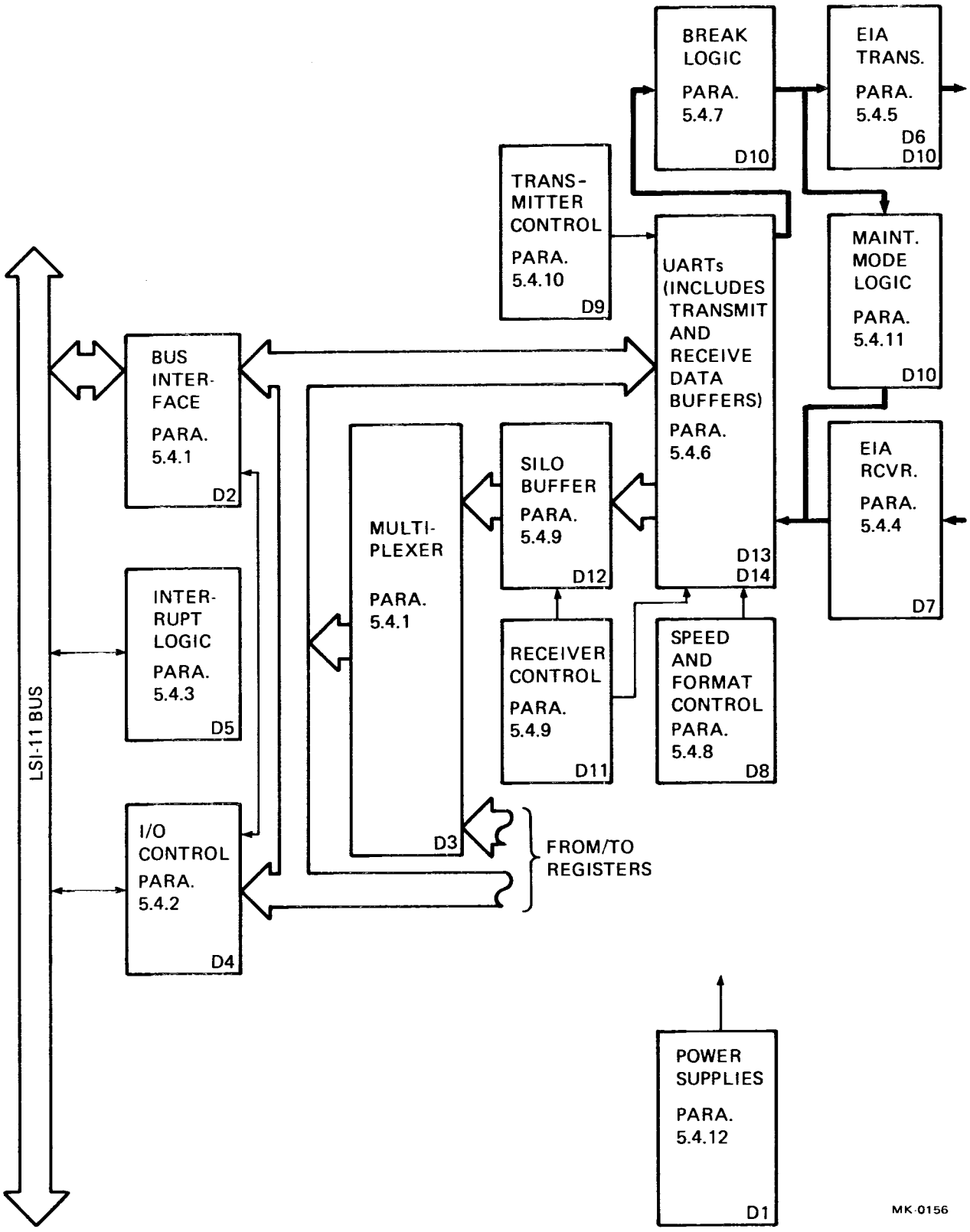


Figure 5-10 Simplified Functional Block Diagram

The speed and format control generates clock signals for the UARTs. Under program control, it selects baud rate and stop bit, parity bit and character length parameters.

The break logic inhibits output data to create a BRK signal. The four lines operate independently and under program control.

The maintenance mode data selector provides the capability of switching the data outputs the data inputs. This is used to verify module operation.

The power supplies convert voltages available on the LSI-11 bus into other voltages also required by the module.

Each of the circuits shown in Figure 5-10 is described in greater detail in Paragraph 5.4.

5.4 CIRCUIT OPERATION

The interaction between the LSI-11 and the DZV11 is asynchronous to the interchanges between the DZV11 and the communication lines it controls. Therefore, the circuit description in this paragraph treats the module from three points of view. Paragraphs 5.4.1 through 5.4.3 cover the operations of moving control, status, and character data between the LSI-11 and the DZV11 internal registers. Paragraphs 5.4.4 through 5.4.7 discuss the flow of data between the external lines and the DZV11 internal registers. Paragraphs 5.4.8 through 5.4.11 discuss functions that are controlled by the computer but directly affect the movement of data between the DZV11 and the lines. Paragraph 5.4.12 discusses the power supplies.

5.4.1 Bus Interface

Data and control signals move between the LSI-11 bus and the DZV11 transmit and receive circuitry by means of a group of bus transceivers, multiplexers, and latches. Figure 5-11 indicates the functional relationship of these circuits to the addressable device registers.

The bus transceivers are contained in four DC005 transceiver chips. These interface LSI-11 bus lines BDAL00 through BDAL15 to the module's internal device data bus lines 00 through 15. The device data bus lines have three logical conditions: TTL low, TTL high, and disabled. The disabled state is a very high impedance, which permits the internal bus lines to be used in both directions by high-speed, low-power devices.

The transceiver chips also perform the functions of address decoding and vector generation. Address decoding is accomplished by comparing the states of BDAL03 through BDAL12 with the states selected by address switches A03 through A12 (switches 10 through 1, respectively, on switchpack E30). When the LSI-11 addresses an I/O device, it asserts BBS7 L (bank select 7) during address time. This indicates that the address is in the 28K–32K range of addressing space, and enables the DC005 transceivers to decode the address. If the address matches the switch selection, the circuit asserts DEVICE SELECT H to the I/O control logic.

During data time, the transceivers transfer data from the LSI-11 bus lines to the device data bus lines if the operation is an output data transfer. If the operation is an input data transfer, the I/O control logic asserts READ L and READ DEVICE H. This switches the transceivers to their opposite state, in which they transfer data from the device data bus to the LSI-11 bus.

The bus interface logic generates vector addresses under the control of the interrupt logic and vector address switches V03 through V08 (switches 6 through 1, respectively, on switchpack E2). The vector switches set the states of vector bits 03 through 08 when the interrupt logic enables vector generation. Bit 02 is controlled directly by the interrupt logic. It is set for a transmitter interrupt and cleared for a receiver interrupt.

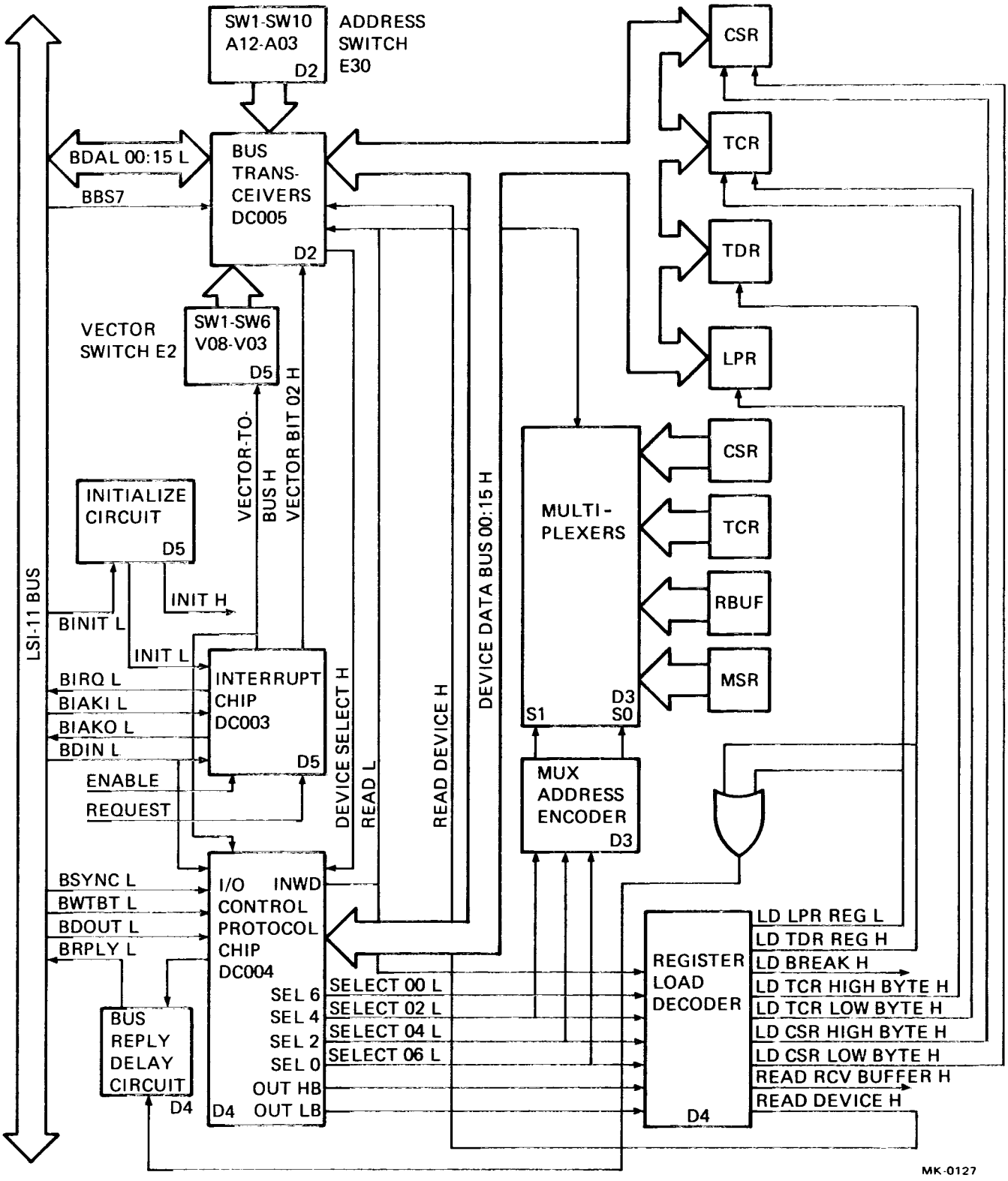


Figure 5-11 Bus Interface, I/O Control and Interrupt Logic

When an interrupt occurs, the conditions selected by the vector switches are immediately placed on the LSI-11 bus lines. The transceivers do this without need of READ L or READ DEVICE H from the I/O control circuit.

5.4.2 I/O Control

The I/O control logic controls the flow of status bits and data bits between the LSI-11 and the device registers. It monitors the three least significant bits of the address word to determine which register is to be read or loaded, and which byte in the register is affected. It monitors BWTBT L (Write Byte) to determine if a byte is being loaded or a word is being loaded. (The LSI-11 can write bytes, but reads only words.) Control signals BDIN L and BDOUT L indicate whether data is to be moved into the computer or out of it.

The major element in the I/O control circuit is a DC004 protocol chip (Figure 5-11). The chip uses device data bus bits 01 and 02 to decode the device register address and then asserts one of four register select lines. It uses device data bus bit 00 and BWTBT L to select either OUT HB for a high byte or OUT LB for a low byte. If the operation is an output data transfer (indicated by BDOUT L), the register load decoder uses OUT LB, OUT HB (or both) and the register select signals to produce a load pulse. The load pulse enables the proper byte or bytes of the selected register to be loaded from the device data bus.

The register select lines are also used to control the address lines on a group of eight multiplexers. If the operation is an input data transfer (indicated by BDIN L), the I/O control switches the multiplexers to the selected register and asserts READ L and READ DEVICE H. READ L enables the multiplexers to place the data from the selected register on to the device data bus (Table 5-3). READ L and READ DEVICE H together enable the bus transceivers to transfer the data from the device data bus to the LSI-11 bus (Table 5-4).

Table 5-3 Multiplexer Addressing

SELECT L*			MUX		Selected Register
06	04	02	S1	S0	
F	F	F	F	F	CSR
F	F	T	F	T	RBUF
F	T	F	T	F	TCR
T	F	F	T	T	MSR

*T = TRUE condition, that is, +3 V on signal lines with an H suffix and 0 V on signal lines with an L suffix.

Table 5-4 Transceiver Switching

READ L*	READ DEVICE H	Mode
F	F	LSI-11 bus to device data bus
F	T	Does not occur
T	F	LSI-11 bus disconnected/device data bus open
T	T	Device data bus to LSI-11 bus

*T = TRUE condition, that is, +3 V on signal lines with an H suffix and 0 V on signal lines with an L suffix.

5.4.2.1 Input Operation – An input data transfer (DATI bus cycle) proceeds as follows.

1. The CPU places the device address on LSI-11 bus lines BDAL00 L through BDAL15 L, and asserts BBS7 L. BWTBT L is negated at this time because all input transfers are full words (Figure 5-12).

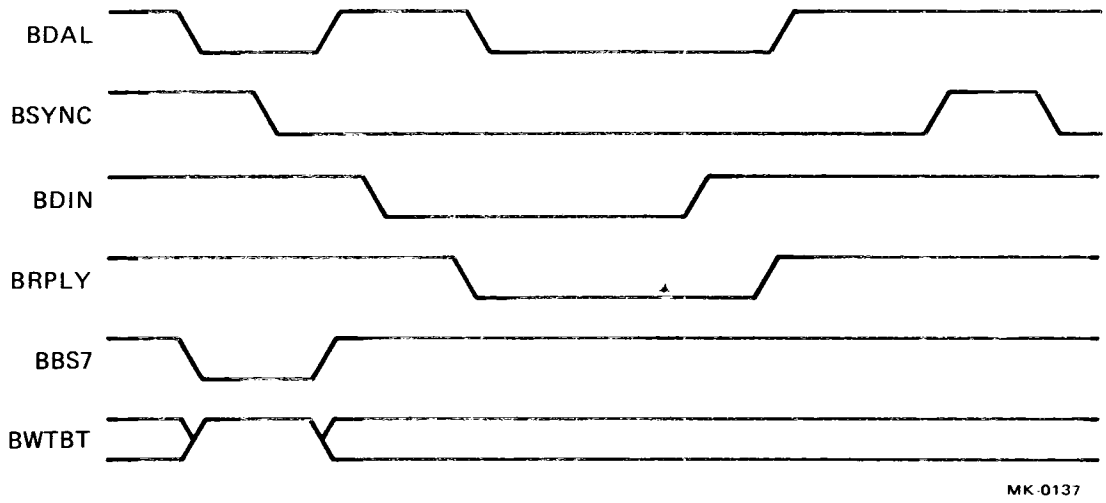


Figure 5-12 Data Input Timing

2. The bus transceivers are configured to receive from the LSI-11 bus unless switched otherwise. BBS7 L enables the transceivers to decode the address and to assert DEVICE SELECT H, which enables the I/O control circuit.

3. The CPU asserts BSYNC L. The leading edge of BSYNC L latches the states of DEVICE SELECT H and device data bus bits 00 through 02 into the protocol chip. These are decoded to select the desired register by addressing the multiplexers.

4. Next, the CPU removes the address from the LSI-11 bus lines, negates BBS7 L, and asserts BDIN L. BDIN L causes the I/O control to generate READ L and READ DEVICE H. These signals place the contents of the selected register on the device data bus and the LSI-11 bus. BDIN L also generates BRPLY L. This signals the computer that the data is on the bus.

5. The computer reads in the data and then negates BDIN L.

6. The I/O control logic responds to the negation of BDIN L by negating BRPLY L.

7. The CPU terminates the bus cycle by negating BSYNC L.

8. In the absence of a TRUE condition on BSYNC L, the protocol chip releases the register selection lines and the READ L and READ DEVICE H signals. The bus interface reverts to its normal condition of receiving from the LSI-11 bus and transmitting onto the device data bus.

5.4.2.2 Output Operation – The DZV11 can accept data from the computer in either bytes or words. To write a word out to the module, the CPU performs a DATO bus cycle. To write a byte, it performs a DATOB bus cycle (Figure 5-13). An output data transfer proceeds as follows.

1. The CPU places the device address on the LSI-11 bus and asserts BBS7 L and BWTBT L. (During address time, BWTBT L is asserted for an output operation and negated for an input operation.) BBS7 L enables the bus interface to decode the address and assert DEVICE SELECT H to the I/O control. The bus interface also applies address bits 00 through 02 to the I/O control.

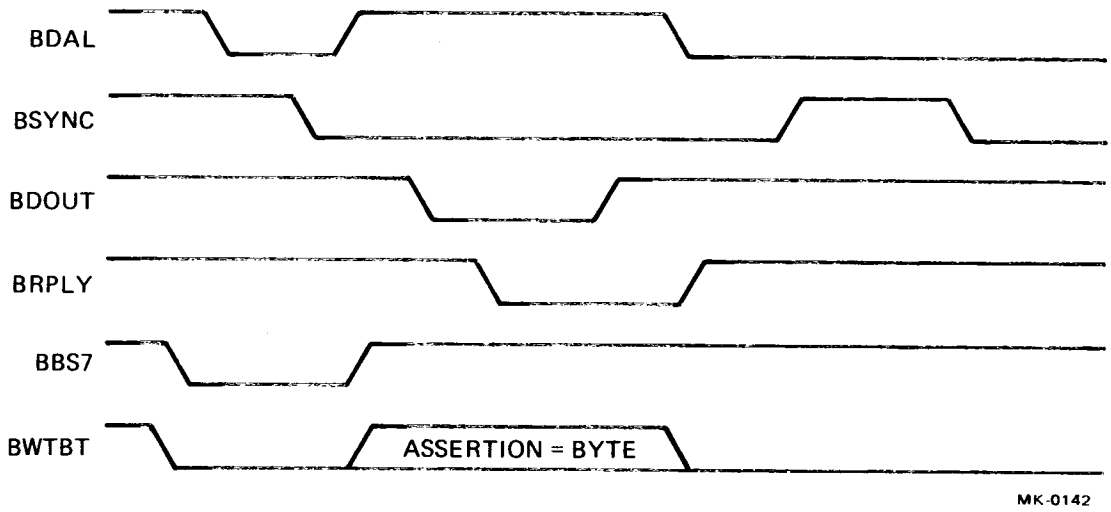


Figure 5-13 Data Output Timing

2. The CPU asserts BSYNC L. The leading edge of BSYNC L latches the states of DEVICE SELECT H and bits 00 through 02 into the protocol chip. The chip decodes the register address and asserts the appropriate select line.

3. The CPU removes the address from the bus lines and negates BBS7 L. If a byte is to be transferred, BWTBT L remains asserted. If a word is to be transferred, BWTBT L is negated.

4. At this time, the CPU asserts BDOUT L. BDOUT L enables the protocol chip to decode the states of BWTBT L and the latched-in address bit 00. The chip uses the signals to assert OUT HB, OUT LB, or, for word transfers, both (Table 5-5). These signals are gated with the select lines to produce a load pulse (or pulses) for the selected byte(s).

5. After the protocol chip receives BDOUT L, it initiates the Bus Reply signal. If the register being loaded is the LPR or the TDR, the Bus Reply signal is delayed before going to the CPU as BRPLY L. The delay ensures a minimum of 300 ns setup time for the register being loaded. The LPR and TDR are located inside the UART and baud rate generator chips, and therefore require longer to set up than the high-speed latches comprising the other registers.

   After the delay times out, BRPLY L is asserted to the CPU to indicate that the register is loading data.

Table 5-5 Byte Selection (Output Operations Only)

BWTBT L	Device Data Bus Bit 00	Signals Asserted	Bytes Selected
F	Don't care	OUT LB L and OUT HB L	Both
T	F	OUT LB L	Low
T	T	OUT HB L	High

6. Next, the CPU removes the data from the bus lines and negates BDOUT L.
7. The protocol chip responds to this by negating BRPLY L.
8. The CPU then terminates the bus cycle by negating BSYNC L and, if applicable, BWTBT L.
9. When BSYNC L is negated, the protocol chip negates the register select and byte lines.

5.4.2.3 Vector Operation – The I/O control has the additional function of asserting BRPLY L in response to VECTOR-TO-BUS H from the interrupt control circuit. This action is part of the interrupt sequence, and is independent of the BSYNC L and DEVICE SELECT H. It is discussed in Paragraph 5.4.3.

5.4.2.4 Initialize Circuit – This circuit produces two initialization signals (INITIALIZE H and INITIALIZE L) when it receives either BINIT L from the LSI-11 bus or the Master Clear bit from the CSR. Both input signals also generate other clear signals (Figure 5-14). The initialization and clear signals clear the registers and latches on the module to set initial conditions.

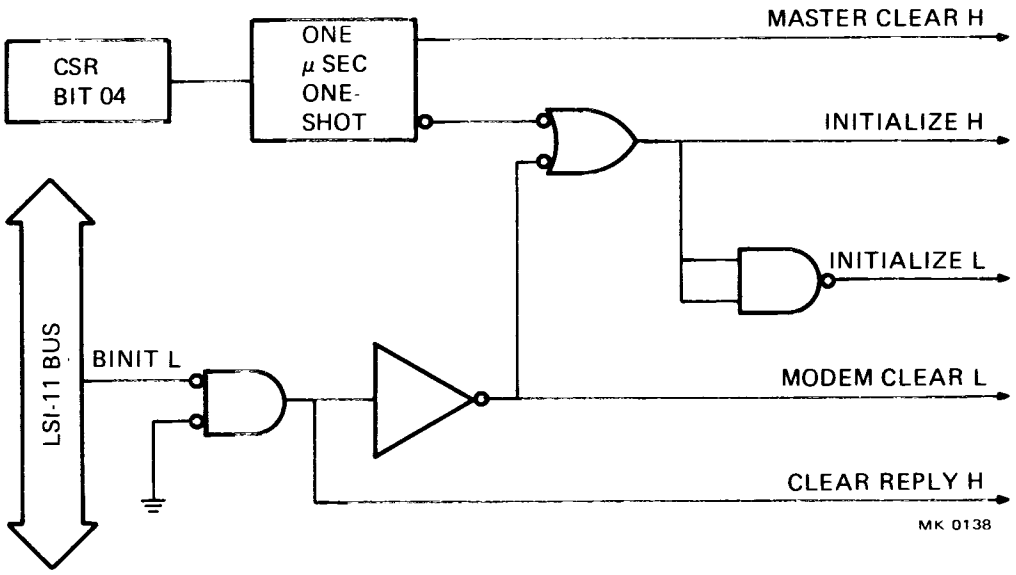


Figure 5-14 Initialization Signals

5.4.3 Interrupt Logic

Most of the logic for interrupts is contained in a single DC003 interrupt chip (Figure 5-15). The chip contains two interrupt channels: one for receiver interrupts and one for transmitter interrupts. The circuit generates a receiver interrupt either when the RBUF has one character ready for the computer (Receiver Done interrupt) or when the silo buffer has 16 characters ready (Silo Alarm interrupt).

The Receiver Done interrupt is enabled by setting CSR bit 06. The Silo Alarm interrupt is enabled by setting bit 12. Setting bit 12, however, inhibits the receiver done signal from the RBUF. Therefore, Receiver Done interrupts do not occur when Silo Alarm interrupts are enabled.

The circuit generates a transmitter interrupt when the TDR is empty and ready for another data output from the computer. The Transmitter Ready interrupt is enabled by setting CSR bit 14.

Both the TIE and RIE bits are located physically in the DC003 interrupt chip although they are functionally part of the CSR.

The LSI-11's Interrupt Acknowledge signal (BIAKI L/BIAKO L) is daisy-chained through the devices on the LSI-11 bus. A device priority is established by its position in the Interrupt Acknowledge daisy-chain. In the DZV11 interrupt logic, the chain goes through both the receiver section and the transmitter section of the interrupt chip. It passes through the receiver section first, thereby giving receiver interrupts priority over transmitter interrupts.

Backplanes that provide bussed LSI-11 signals to the C and D sections of the module also use the daisy-chain scheme in the C section. Jumpers W10 and W11 on the DZV11 pass the Interrupt Acknowledge and DMA Grant signals to prevent breaking the chain in that section of the backplane.

5.4.3.1 Interrupt Transactions – When interrupts are enabled and a condition requiring service occurs, the interrupt sequence proceeds as follows.

1. The interrupt logic asserts BIRQ L, the interrupt request line (Figure 5-16).

2. The LSI-11 responds to BIRQ L by asserting BDIN L and then BIAKI L. BIAK is the bussed Interrupt Acknowledge signal. It is passed down the priority chain until it reaches the section of the interrupt chip that initiated the request.

3. When the interrupt logic receives both BDIN L and BIAKI L, it asserts VECTOR-TO-BUS H to the vector selection switches. If the interrupt is a transmitter interrupt, the circuit also asserts VECTOR BIT 02 H. This signal adds four to the base (receiver interrupt) vector that is asserted by VECTOR-TO-BUS H. The circuit also negates BIRQ L.

4. VECTOR-TO-BUS H causes the I/O control logic to issue BRPLY L to the LSI-11. VECTOR-TO-BUS H and, if applicable, VECTOR BIT 02 H cause the bus transceivers to place the selected vector on the LSI-11 bus lines.

5. The computer reads in the interrupt vector and then, as a result of receiving BRPLY L, negates BDIN L. Shortly after this, it also negates BIAKI L.

6. The interrupt logic negates VECTOR-TO-BUS H and, if applicable, VECTOR BIT 02 H.

7. The negation of VECTOR-TO-BUS H causes the I/O control logic to negate BRPLY L, and the bus transceivers to remove the vector from the LSI-11 bus lines.

An interrupt transaction does not require BBS7 L, DEVICE SELECT H, BSYNC L, or READ L. The interrupt logic overrides the normal I/O protocol.

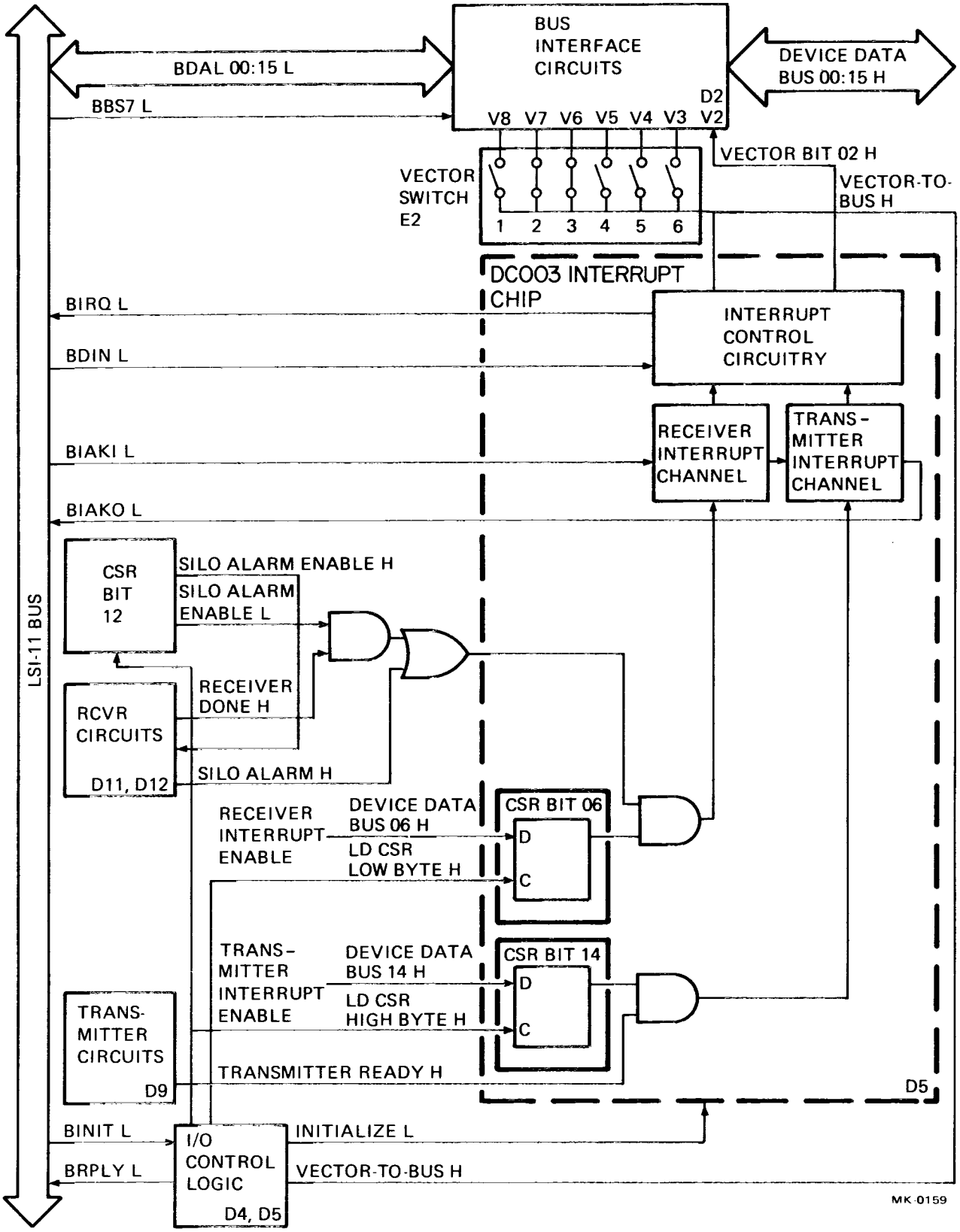


Figure 5-15 Interrupt Logic

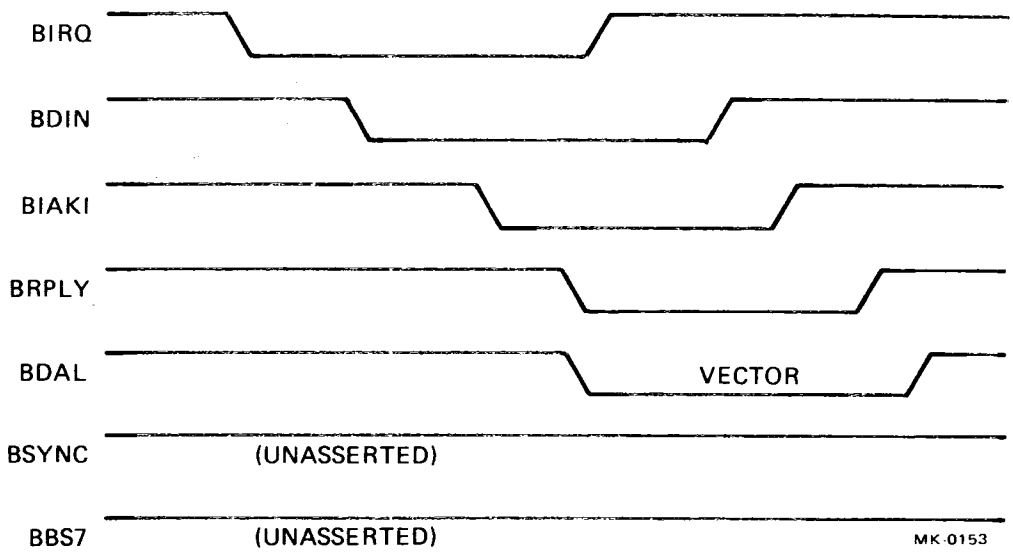


Figure 5-16 Interrupt Timing

A Silo Alarm interrupt can be distinquished from a Receiver Done interrupt by checking SAE bit (CSR bit 12) when entering a service routine.

5.4.4 EIA Receivers

The DZV11 receives three modem signals for each of the four communicaton lines it interfaces. Carrier Detect, Ring Indicator, and Received Data are received and converted from EIA levels to TTL levels. The Carrier and Ring signals go to the modem status register. The received data signals go to the RBUF (in the UARTs). Refer to Figure 5-17.

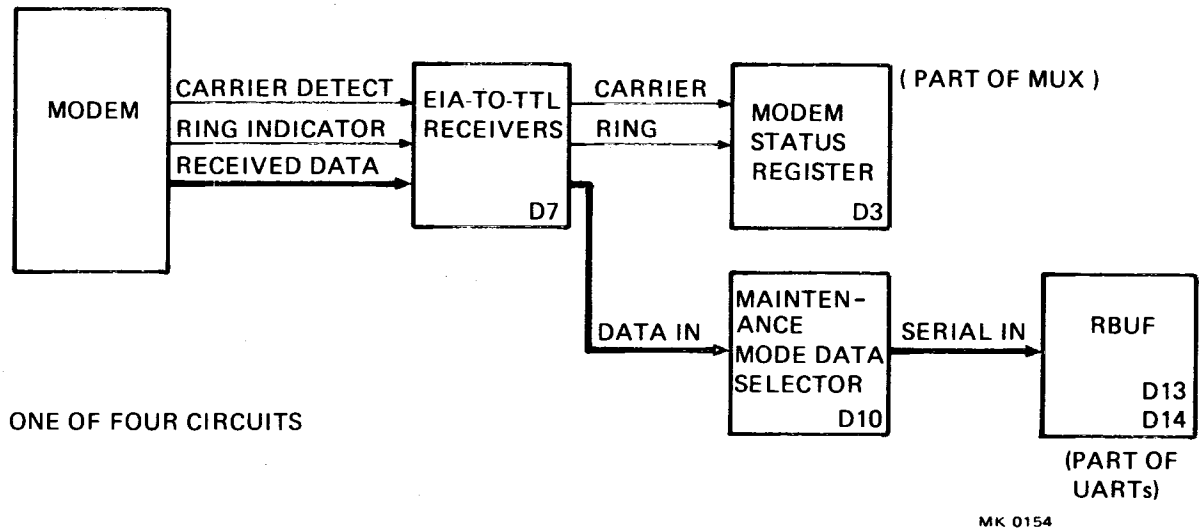


Figure 5-17 EIA Receivers

5.4.5 EIA Transmitters

The DZV11 can control up to three modem control signals for each of the four communications lines it interfaces (Figure 5-18). Control bits from the TCR are converted from TTL levels to EIA levels to drive modem control lines. For each line there is a single control bit that is always connected to data terminal ready (DTR). These signals may be jumpered to also control request to send (RTS). If this done, they may then be further jumpered to control forced busy (for Bell model 103E and 113B modems with the forced busy option).

Data to be transmitted from the computer to the lines moves from the transmitter data buffer to the EIA transmitters, where it is converted from TTL levels to EIA levels and placed on the lines.

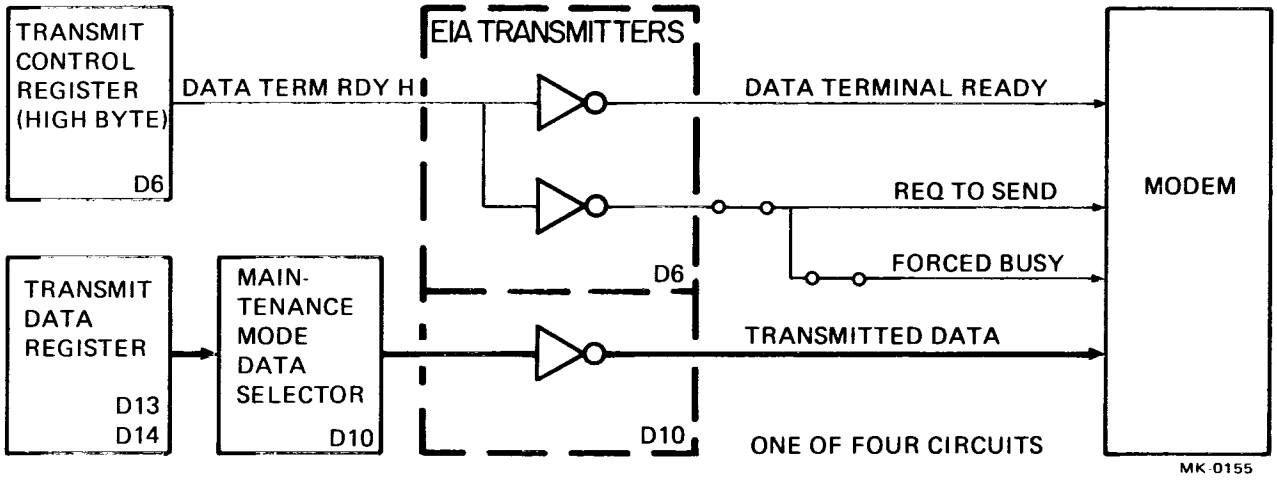


Figure 5-18 EIA Transmitters

5.4.6 UARTs

The DZV11 uses four UART chips, one for each of the four communication lines. Each UART performs part of the functions of receiver buffer (RBUF), transmitter data register (TDR), and line parameter register (LPR) for the channel under its control. The RBUF takes serial data received by the EIA receivers, strips off the start, stop, and parity bits, converts it to parallel data, stores it in the silo buffer, and then places it on the device data bus. The TDR takes parallel data from the device data bus, appends start, stop, and parity bits, converts it to serial data, and sends it to the EIA transmitters. The LPR controls the speed, parity, and number of stop bits that the RBUF and TDR use. (Figure 5-19).

5.4.6.1 Setting Line Parameters – The various formats and speeds available are described in Paragraph 1.3.3 (Performance). The names and meanings of the LPR bits are listed in Table 3-4. The low byte of the LPR is contained inside the UARTs, and controls the data format. The high byte is contained in the baud rate generator circuits, and controls the speed at which data is transmitted and received.

When the computer addresses the LPR, the I/O control logic generates a load pulse. The load pulse enables the LPR bits 00 and 01 to strobe the selected UART and baud rate generator. Bits 03 through 07 are latched into the UART to select the data format. Bits 08 through 11 are latched into the baud rate generator to select the speed. Bit 12 enables the Receiver Clock signal to reach the UART.

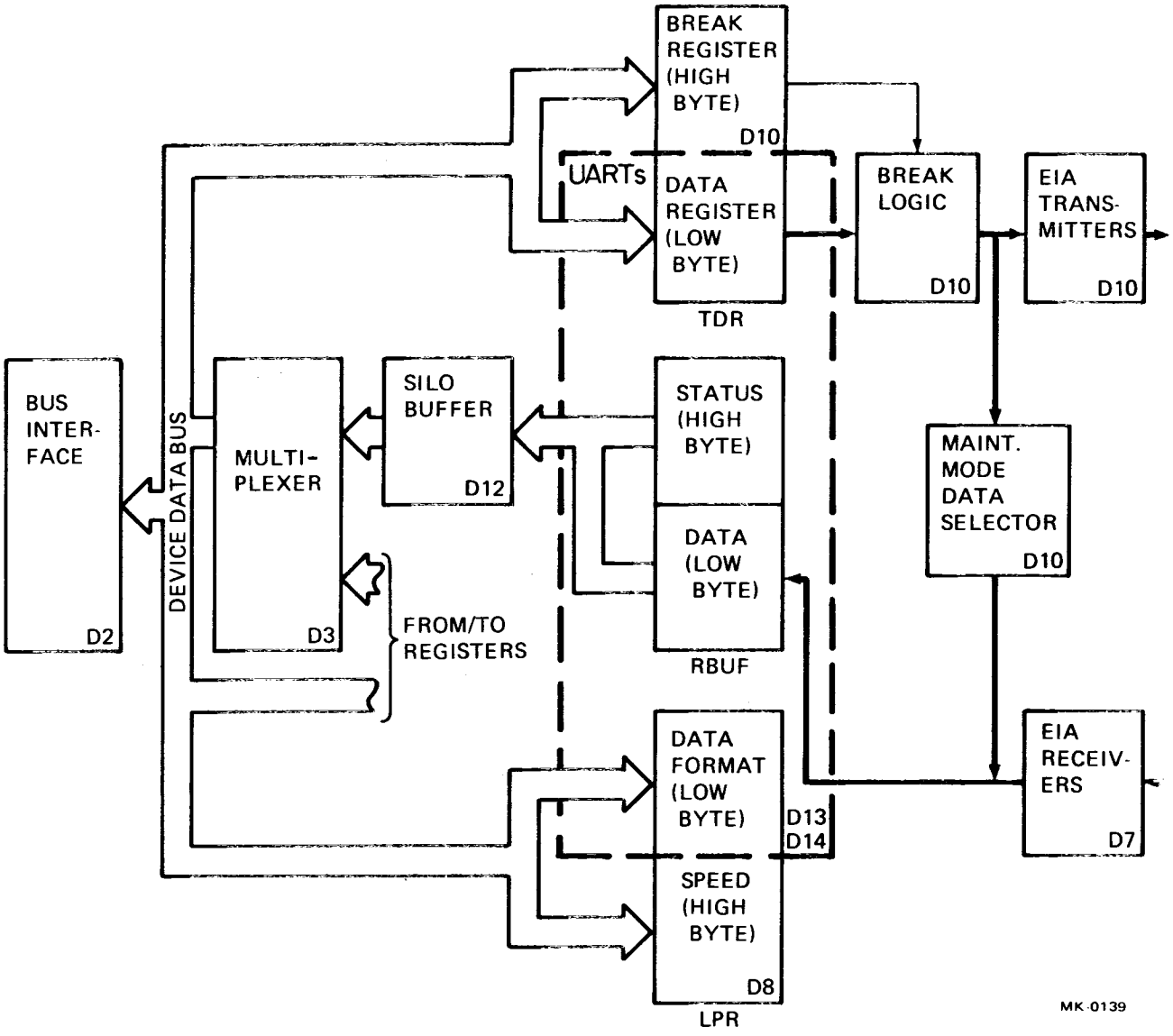


Figure 5-19 UARTs

5.4.6.2 UART Receiver Operation – Serial data coming in from the EIA receiver is applied to the receiver section of the selected UART. The UART samples the serial input at the receiver clock rate (16 times the data bit rate). The line is in a continuous marking state when idle. When a start bit arrives, the UART detects the mark-to-space transition. It samples the line again at the time corresponding to the middle of the start bit. If the line is marking, the UART logic assumes that the first sample was noise, and resumes sampling. If it finds that the line is still spacing, however, the logic assumes it is receiving a start bit, and enters the data entry mode. In this mode, the UART shifts the data serially into an internal register (Figure 5-20). If parity is enabled, the UART checks the total of the received data bits plus the parity bit. (It checks for an even total if even parity has been selected, and an odd total if odd parity has been selected.) A parity error causes the UART to set the parity error flag bit in the high byte of the RBUF word.

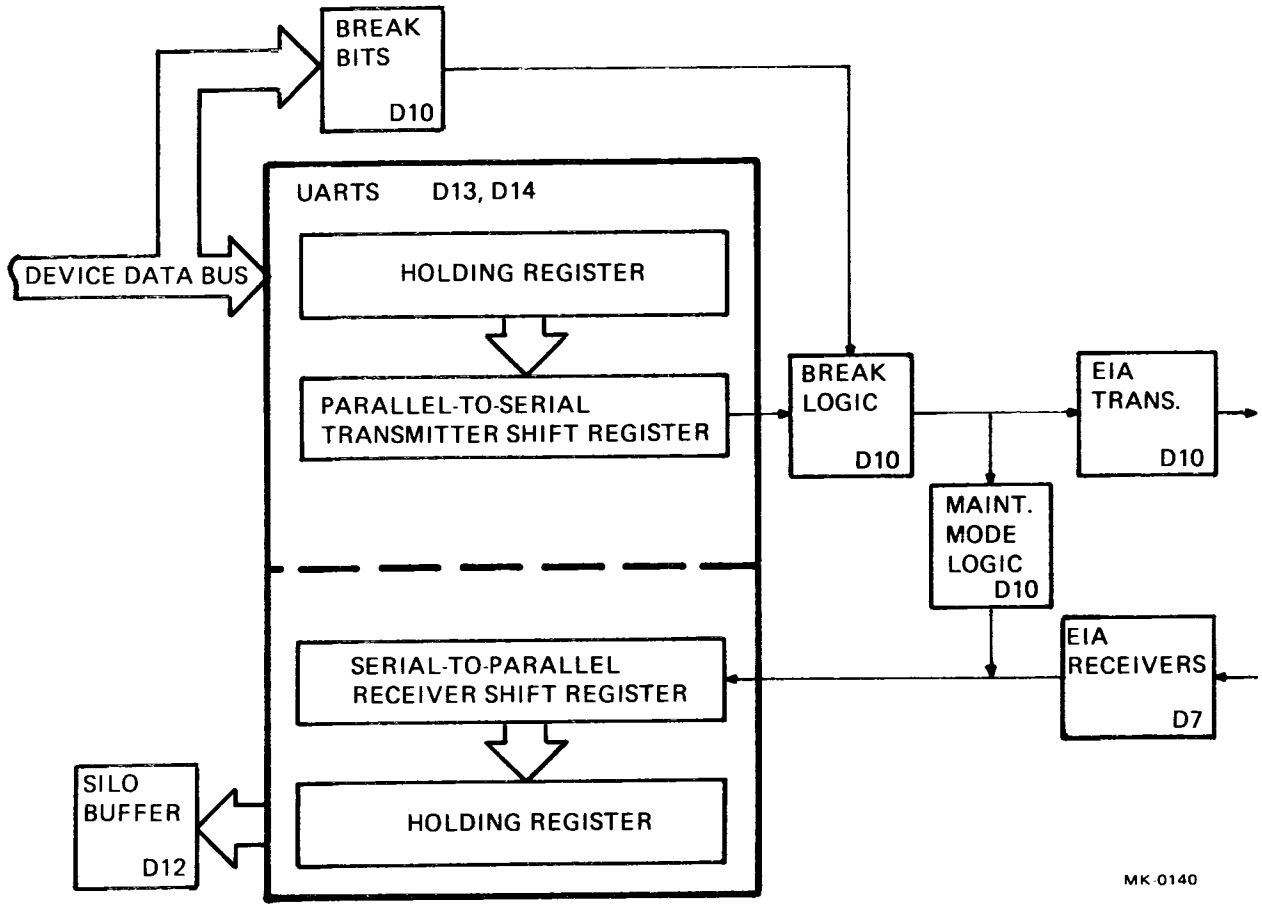


Figure 5-20 UART and Break Bit Registers

The UART checks the stop bit to see if it is marking. If the line is spacing instead, the UART sets the framing error flag bit. If the line is marking, the UART logic assumes there is a valid stop bit.

About half way through the stop bit time, the UART transfers the received character data, the parity error bit, and the framing error bit from the serial shift register to the holding register. At this time it asserts the Data Available signal to the receiver control logic. If the previous character has not yet been serviced by the receiver control logic, the UART sets the overrun error flag bit to indicate that the previous character was lost.

The receiver control loads the contents of the RBUF (data and status) into the silo buffer for subsequent transfer to the computer. The receiver control circuit determines when and what type of receiver interrupt to request.

5.4.6.3 UART Transmitter Operation – During idle time, the UART transmits a continuous marking signal and holds the Transmitter Ready (TBMT) signal asserted. The transmitter control circuitry uses this signal to determine when to initiate a transmitter interrupt request.

When the computer has data to transmit to a communication line, it uses a DATO or DATOB sequence to address the TDR and place the data on the bus lines. The low byte of the TDR word is loaded into a holding register in the UART. When the data enters the holding register, the UART negates TBMT. It then transfers the data in parallel from the holding register to a serial shift register and reasserts TBMT. In the serial shift register, the UART attaches start, stop, and parity bits, as set by the LPR. The assembled character is then shifted serially out to the EIA transmitter.

Because the transmitter, like the receiver, is double-buffered, it can be loaded with a second character before the first one moves out.

5.4.7 Break (BRK) Bits

The transmission and reception of BRK bits are closely related to the transmission and reception of data. A Break signal is a continuous spacing condition on the serial data line. When a UART receives a Break signal, it interprets the continuous space as a character that is missing a stop bit. Therefore, it sets the framing error flag. The program then determines how a framing error is handled.

A Break signal may be transmitted by interrupting the flow of serial data leaving the UART. The high byte of the TDR may be thought of as a break register. It contains one BRK bit for each of the four communication channels. Setting one of these bits inhibits the flow of data from the UART transmitter to the EIA transmitter, thereby causing a Break to be transmitted on the communication line. Refer to Figure 5-20.

5.4.8 Speed and Format Control

The circuits controlling speed and format include the LPR, two dual baud rate generator chips, an oscillator, and two addressable latches. Refer to Figure 5-21.

When the LSI-11 computer writes a word out to the LPR, the following events occur.

1. During address time, the bus interface and I/O control circuitry decode the address and produce a load pulse, LD LPR REGISTER L.

2. During data time, the load pulse enables two addressable latches to be addressed by bits 00 through 02. One latch routes the state of bit 12 to a gate that inhibits or enables the receiver clock to the selected UART.

   The other latch applies an enabling signal (CONTROL STROBE) to both the UART and the baud rate generator chip section that control the communication line selected by bits 00 through 02.

3. Bits 03 through 07 are strobed into the selected UART to select the number of data bits; the number of stop bits; and odd, even, or no parity.

4. Bits 08 through 11 are strobed into the selected baud rate generator chip to control the amount by which the 5 MHz oscillator is divided to produce the UART clock signal. Table 4-1 and Paragraph 4.4.1 describe the baud rate selection scheme.

Thus, the LPR is formed by the latches located in the UARTs, baud rate generators, and addressable latches.

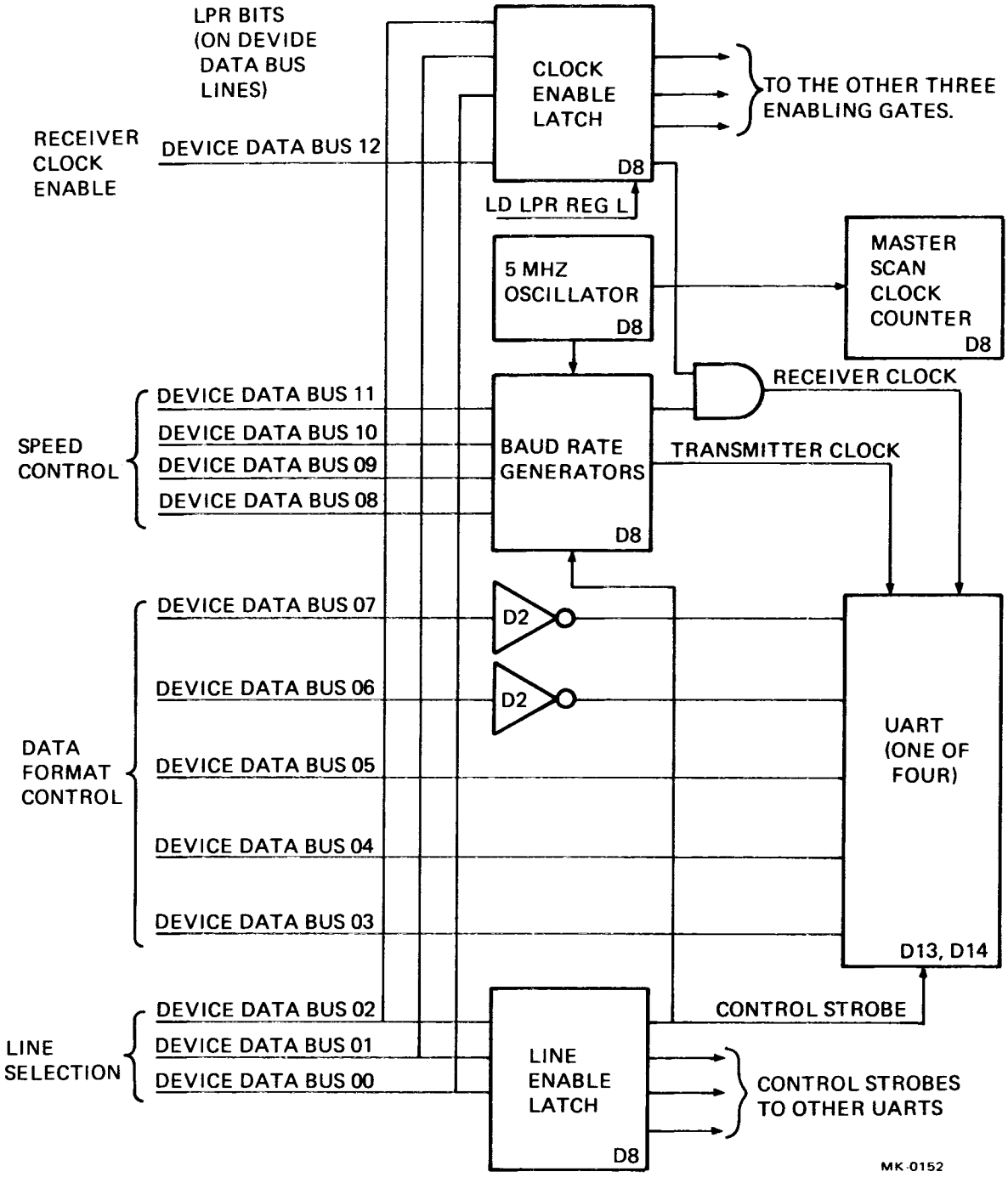


Figure 5-21 Speed and Format Control

5.4.9 Receiver Control

5.4.9.1 Receiver Scanner – The receiver scanner circuit samples the states of the Data Available (DA) signals from the UARTs. When it detects a TRUE condition, it generates a load pulse to transfer the received data from the UART to the silo buffer. The sequence in which the receiver data available flags are scanned and the characters loaded into the silo buffer is controlled by a 4-phase timing sequencer and a group of multiplexers, demultiplexers, and counters.

The sequencer produces four timing signals (Figure 5-22). The signals times are designated Phase 1 through Phase 4.

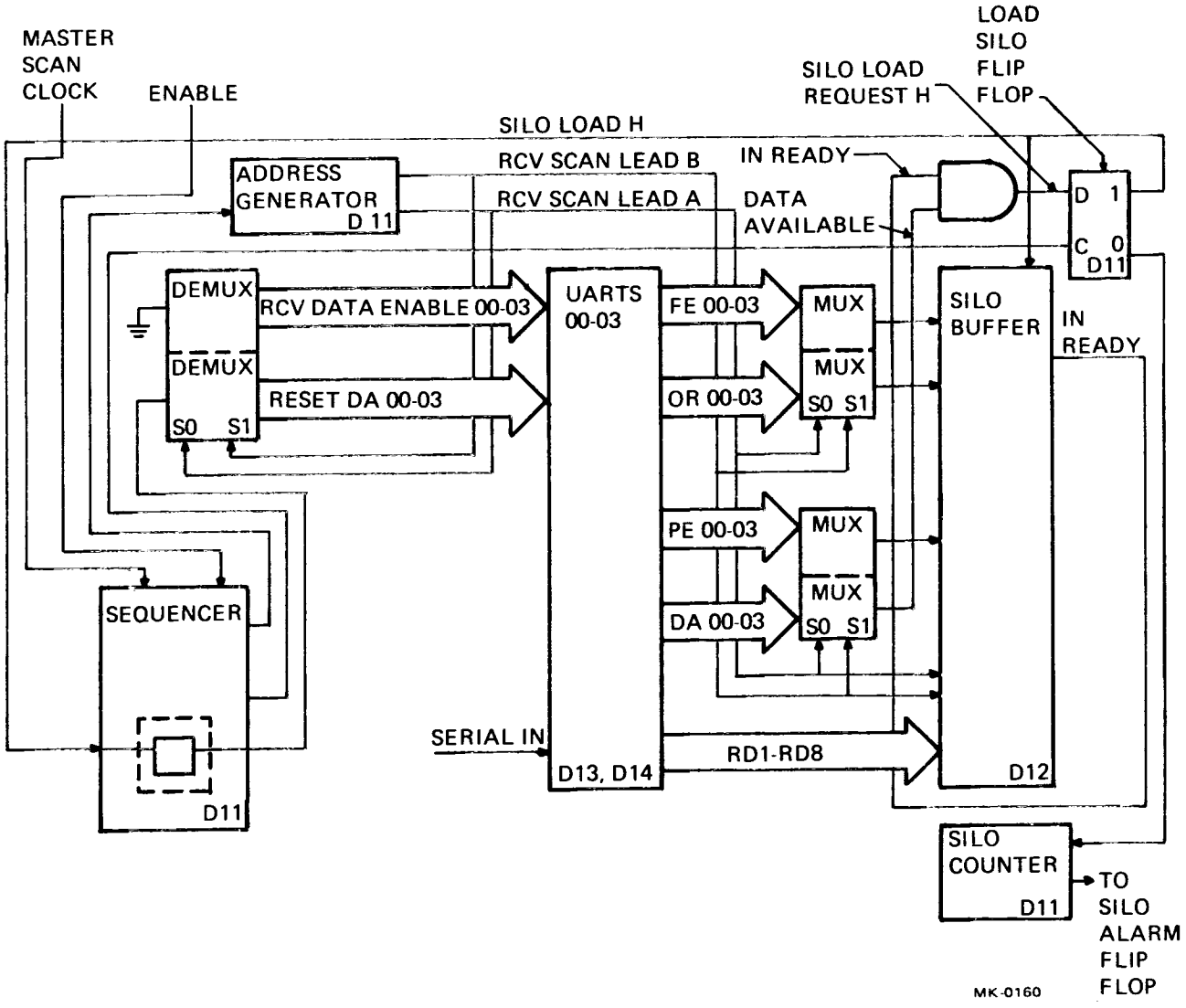


Figure 5-22 Receiver Control

During Phase 1, a signal toggles the address generator to increment by one count. The two least significant bits of the counter are used as a 2-bit address code, designated RCV SCAN LEAD A and RCV SCAN LEAD B. These two signals address a multiplexer. The multiplexer selects the Data Available line from the UART corresponding to the address code and applies it to a gate. The other input to the gate is a Ready signal from the silo buffer. This signal is asserted when the silo buffer is ready to accept data. If the Data Available signal is set and the silo buffer is ready, the gate asserts SILO LOAD REQUEST H. The load request is applied to the load silo flip-flop.

RCV SCAN LEAD A and RCV SCAN LEAD B also address a demultiplexer. The demultiplexer places an enabling signal (RCV DATA ENABLE) on the line to the UART addressed by the scan leads. This is the same UART that is having its Data Available line sampled. The RCV DATA ENABLE signal enables the UART to place the contents of its receiver holding register on the lines to the silo buffer (RD1 through RD8).

During Phase 2, the sequencer clocks the load silo flip-flop. If SILO LOAD REQUEST H is true, the flip-flop sets. When the flip-flop sets, one output goes to the silo buffer as LOAD SILO H and strobes received data from the UART into the silo buffer. At the same time the data enters, status information is also loaded into the silo. Framing Error, Overrun Error, and Parity Error bits from the selected UART are routed via multiplexers into the silo. The states of RCV SCAN LEAD A and RCV SCAN LEAD B are loaded into the silo to indicate which communication line the received character came from.

LOAD SILO H also goes to a latch in the sequencer. From there it passes through a demultiplexer and asserts RESET DA to the selected UART. RESET DA clears the data available flag in the UART so that another character may be received.

At the beginning of Phase 3 time, the zero output of the load silo flip-flop clocks the silo counter. The silo counter increments by one count to keep a tally of the number of times the silo buffer has been loaded. The silo counter counts only when SAE is set.

Phase 4 re-establishes the initial conditions of the scanner circuit for the next scan cycle.

5.4.9.2 Silo Buffer – The silo buffer comprises four 4-X 64-bit 3341 serial memory chips. The chips are arranged as a 16-bit-long, 64-word-deep first in/ first out (FIFO) memory. Data is entered in the "top" of the memory as described in the previous section. The In Ready signal means there is a vacancy in the top word of the memory. Similarly, the Out Ready signal indicates there is a word in the "bottom" of the silo waiting to be shifted out.

The buffer stores full RBUF words. Received character data is stored in the low byte, and receiver status data in the high byte. The buffer shifts data in when it receives LOAD SILO H from the load silo flip-flop, and it shifts data out when it receives UNLOAD SILO H from the unload control (Figure 5-23).

Data is shifted out as a result of either a Receiver Done interrupt or a Silo Alarm interrupt. The presence of an Output Ready signal from each of the four chips asserts RECEIVER DONE H to the interrupt logic. If the Receiver Done Interrupt Enable bit is set, the interrupt logic asserts the Interrupt Request signal to the CPU.

If the Silo Alarm Interrupt Enable bit is set, RECEIVER DONE H is inhibited at the interrupt logic. In this case, a receiver interrupt is not requested until the silo buffer has 16 characters ready. Setting Silo Alarm Enable allows the silo counter to increment each time the silo is loaded. On the sixteenth count, the silo counter overflows, and the Carry Out signal sets the silo alarm flip-flop. The flip-flop, in turn, asserts SILO ALARM H to the interrupt logic.

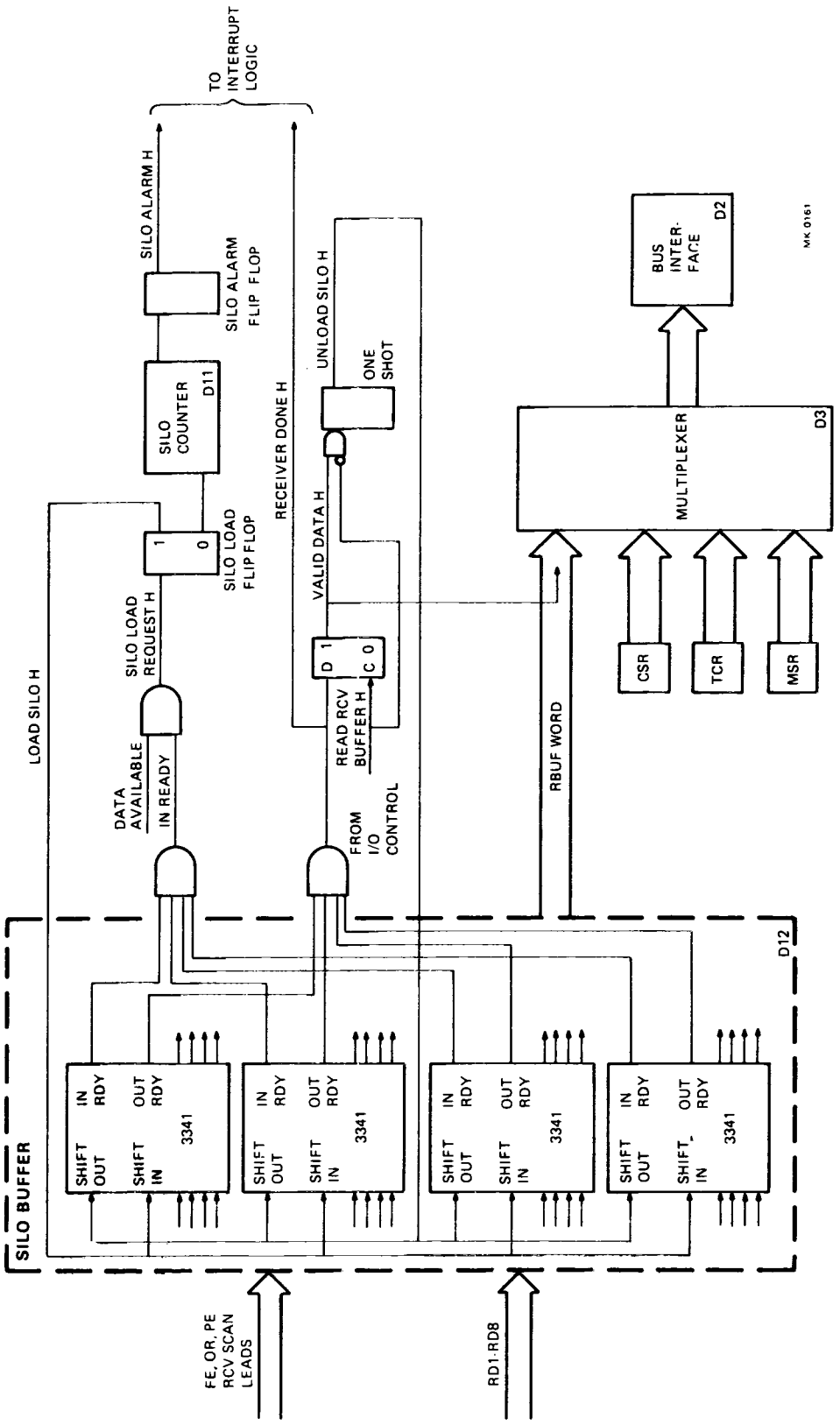


Figure 5-23 Silo Buffer

When the interrupt request is acknowledged, the silo is unloaded. The unloading sequence is the same for both types of receiver interrupts. It proceeds as follows.

1. When data reaches the bottom of the silo, the Out Ready signals are gated together to produce RECEIVER DONE H.

2. RECEIVER DONE H is applied to a latch. When a CPU input transaction (DATI) addresses the RBUF, READ RCV BUFFER H latches the state of RECEIVER DONE H.

3. The output of the latch is VALID DATA H. This signal conditions one input of a one-shot.

4. The trailing edge of READ RCV BUFFER H triggers the one-shot, which generates UNLOAD SILO H.

5. UNLOAD SILO H causes the silo buffer to shift out an RBUF word (character and status data). The word is transferred via a multiplexer to the device data bus. From there the bus transceivers place it on the LSI-11 bus. VALID DATA H is applied to the multiplexer along with the output of the silo buffer, where it becomes bit 15 of the RBUF word.

5.4.10 Transmitter Control

The transmitter control circuit checks the transmitter control register to determine which lines are enabled. It checks the UARTs to determine which are ready to transmit, and it enables the UART controlling the highest priority line to load data from the CPU.

The sequence begins with the Master Scan Enable signal from the CSR (Figures 5-24 and 5-25). MASTER SCAN ENBL H triggers a 350 ns one-shot. The leading edge of the one-shot output clocks a 4-bit latch. A True bit in the latch indicates that the corresponding line is enabled and that the transmitter buffer empty flag is set for the UART controlling that line. Outputs from the latch are applied to a priority encoder. The priority encoder generates a 2-bit code to represent the communication line number. When more than one channel is ready at the same time, the code always indicates the one having the highest priority. (Line 03 has the highest priority; line 00, the lowest.) This code addresses two multiplexers in the transmitter control circuit, and also goes to CSR bits 08 and 09. The CSR bits TLINE A and TLINE B tell the program on which line the next character will be transmitted. The priority encoder also applies a Ready signal to the transmitter ready flip-flop when any of the bits in the latch are true.

The trailing edge of the 350 ns one-shot output performs two functions.

1. The zero (false) output clocks the transmitter ready flip-flop. Assuming a Line Enable bit is set and a TBMT signal is true, the transmitter ready flip-flop asserts TRANSMITTER READY H to the interrupt logic and the CSR. If enabled, a transmitter interrupt request is initiated.

   The transmitter ready flip-flop also disables the gate controlling the input to the 350 ns one-shot. This inhibits further clocking until the line can be serviced. At the same time, the signal enables the contents of the line enable latch to enter a multiplexer.

2. The second function of the trailing edge of the 350 ns one-shot is to trigger a 100 ns one-shot. The output of the 100 ns one-shot disables the input to the 350 ns one-shot. The 350 ns one-shot is inhibited to prevent losing the latched-in line number.

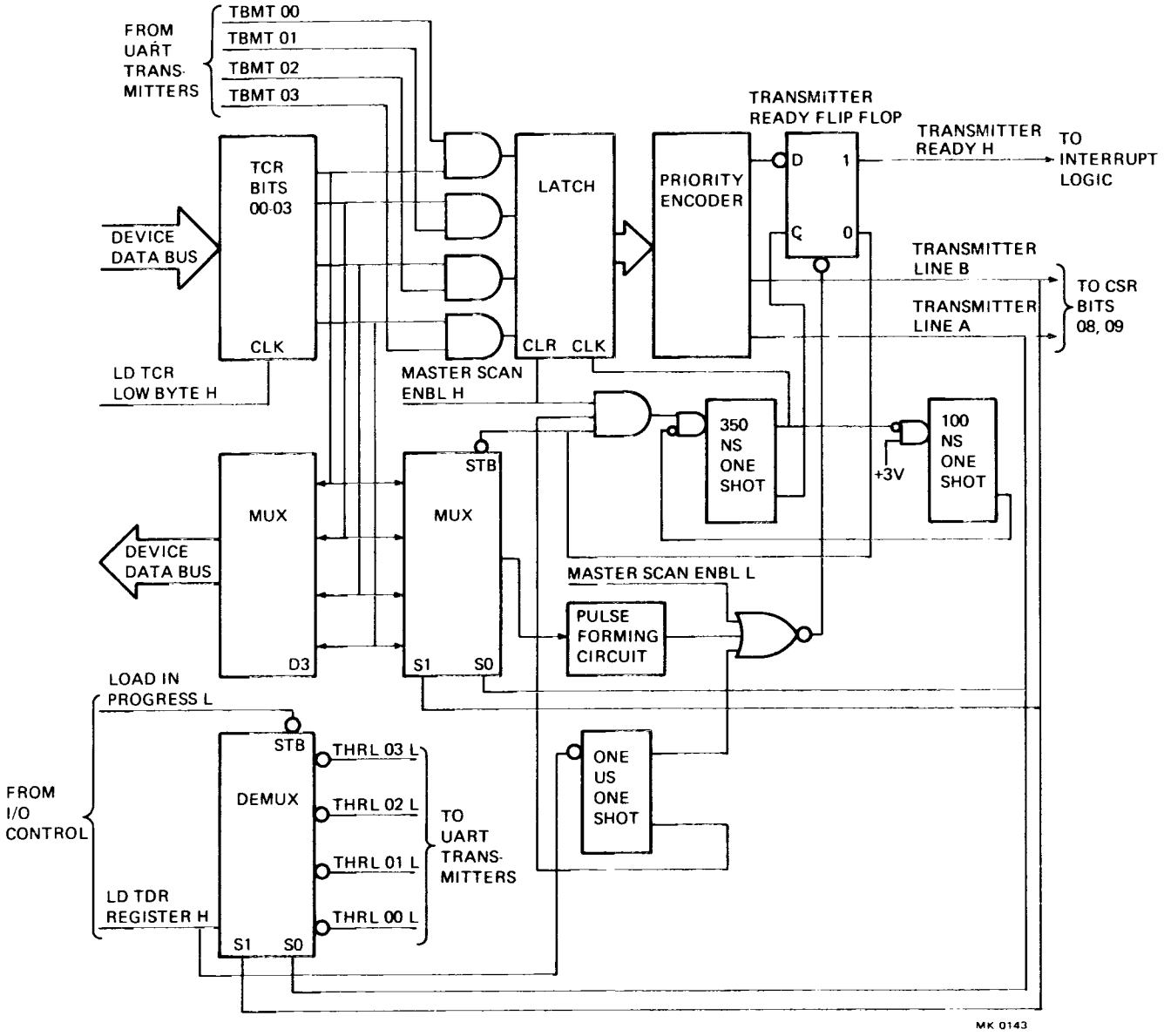
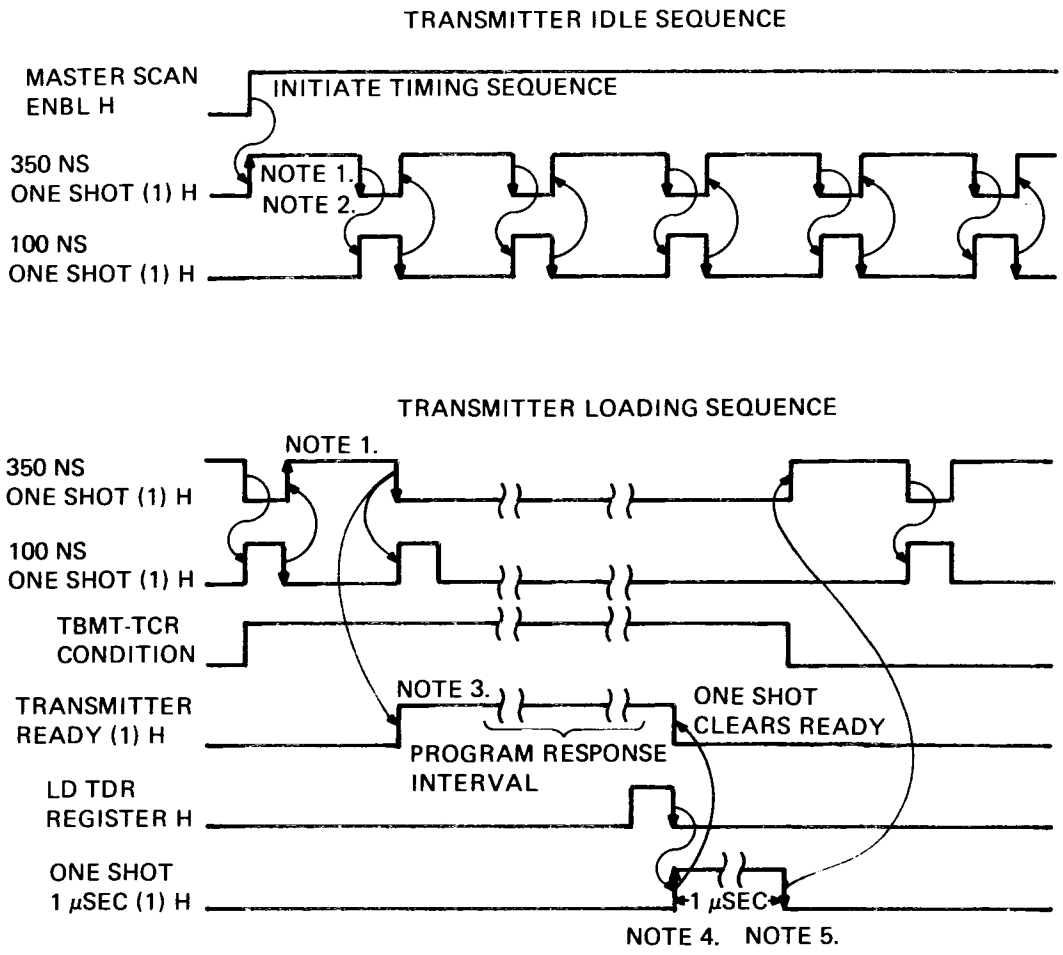


Figure 5-24 Transmitter Control



NOTES:

1. CLOCK EDGE FOR SAMPLING (TBMT•TCR) CONDITIONS.
2. CLOCK EDGE FOR TRIGGERING 100 NS ONE SHOT AND PRESENTING (TBMT•TCR) CONDITIONS.
3. TRANSMIT READY SETS. TIMING SEQUENCE IS DISABLED.
4. POSITIVE EDGE CLEARS TRANSMIT READY AND KEEPS TIMING SEQUENCE DISABLED.
5. FALLING EDGE INITIATES TIMING SEQUENCE FOR NEW SAMPLE.

MK-0151

Figure 5-25 Transmitter Timing

The assertion of TRANSMITTER READY H ultimately results in the CPU performing a DATOB to load data into the TDR. During address time, the I/O control asserts load pulse LD TDR REGISTER H. LOAD IN PROGRESS L from the I/O control strobes LD TDR REGISTER H into a demultiplexer. The demultiplexer output is a transmitter-holding register load pulse (THRL). It is routed to the UART which controls the line addressed by the priority encoder. This enables the UART transmitter to load character data from the device data bus during data time.

When LD TDR REGISTER H returns to the negated state, the trailing edge triggers a 1 μs one-shot. The output of the one-shot clears the transmitter ready flip-flop. It also disables the gate controlling the input to the 350 ns one-shot. The 350 ns one-shot is inhibited in order to allow the UART sufficient time to drop its transmitter buffer empty flag before the circuit starts another scan cycle.

When the program is finished sending a message, it clears the Line Enable bit in the TCR. This occurs after the enable bit and TMBT signals have already been latched in and TRANSMITTER READY H has been asserted. It is, therefore, necessary to prevent the scanner from locking up on a line for which there is no data. This is accomplished by clearing the transmitter ready flip-flop if it is set for a line which is no longer enabled. The states of the Line Enable bits from the TCR are applied to a multiplexer. The bit corresponding to the line addressed by the priority encoder is passed to a pulse-forming circuit. When the bit is cleared, a 50 ns pulse is formed. This pulse clears the transmitter ready flip-flop, thereby negating TRANSMITTER READY H and allowing the 350 ns one-shot to fire for the next transmitter scan cycle.

5.4.11 Maintenance Mode

The DZV11 can be switched to receive the data that it is transmitting (Figure 5-26). The four serial data lines leaving the UARTs are applied to both a data selector and the EIA transmitters. The data selector controls the inputs to the UART receivers. During normal operation, data from the EIA receivers is routed through the data selector to the UART receivers. In the maintenance mode, the data selector ignores the inputs from the EIA receivers. Instead, it routes the output data to the UART receivers. This internal "wrap-around" feature is enabled by setting the Maintenance bit in the CSR. Setting CSR bit 03 asserts MAINTENANCE H, which switches the data selector. External maintenance configurations are discussed in Chapter 6.

5.4.12 Power Supplies

In addition to the +12 V and +5 V available on the LSI-11 bus, the DZV11 also requires +3 V, -9 V, and - 12V. The +3 V source is a voltage divider. The negative voltages are produced by two capacitive charge pump circuits.

Each of the two charge pumps uses the following scheme.

1. An oscillator running at approximately 500 kHz switches a pair of drivers on and off (Figure 5-27).

2. The outputs of the drivers are capacitively coupled to a rectifier.

3. The negative-going output of the rectifier builds up a charge on a capacitor.

4. The charge is Zener-regulated back to the required negative voltage.

5.5 SUMMARY OF DEVICE REGISTERS

This paragraph contains drawings that relate the bits in each register to the circuits in which they are used. Each bit is represented by a block containing the information shown in Figure 5-28. For a description of the meanings and functions of the bits, refer to Chapter 3. For a discussion of their usage, refer to Chapter 4.

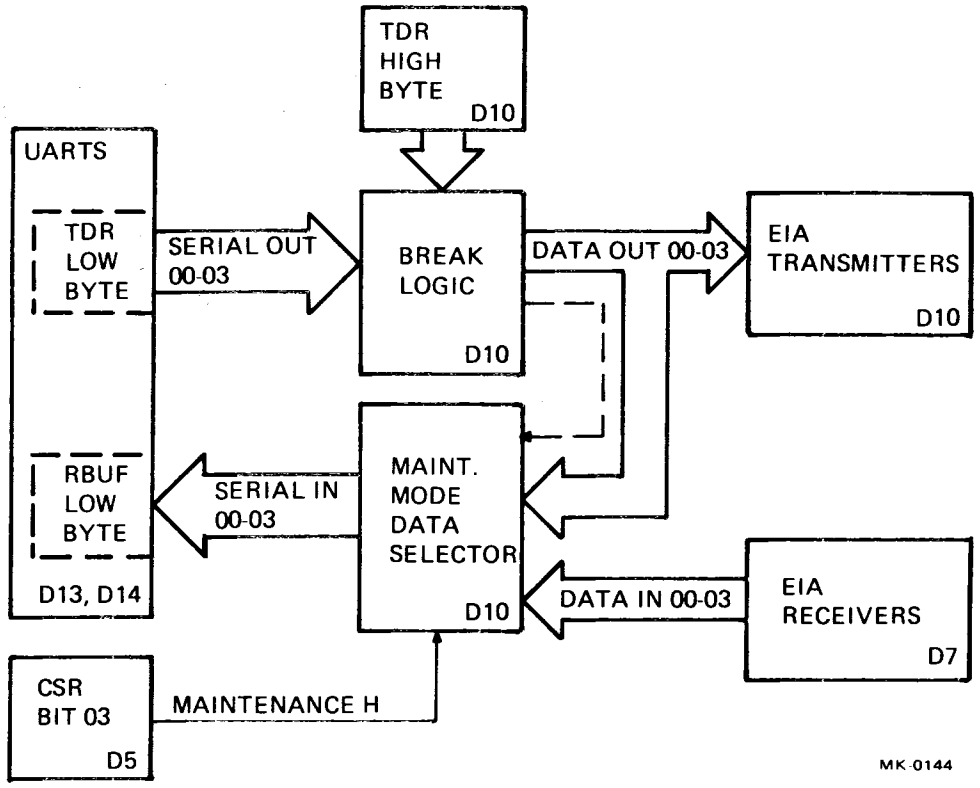


Figure 5-26 Maintenance Mode

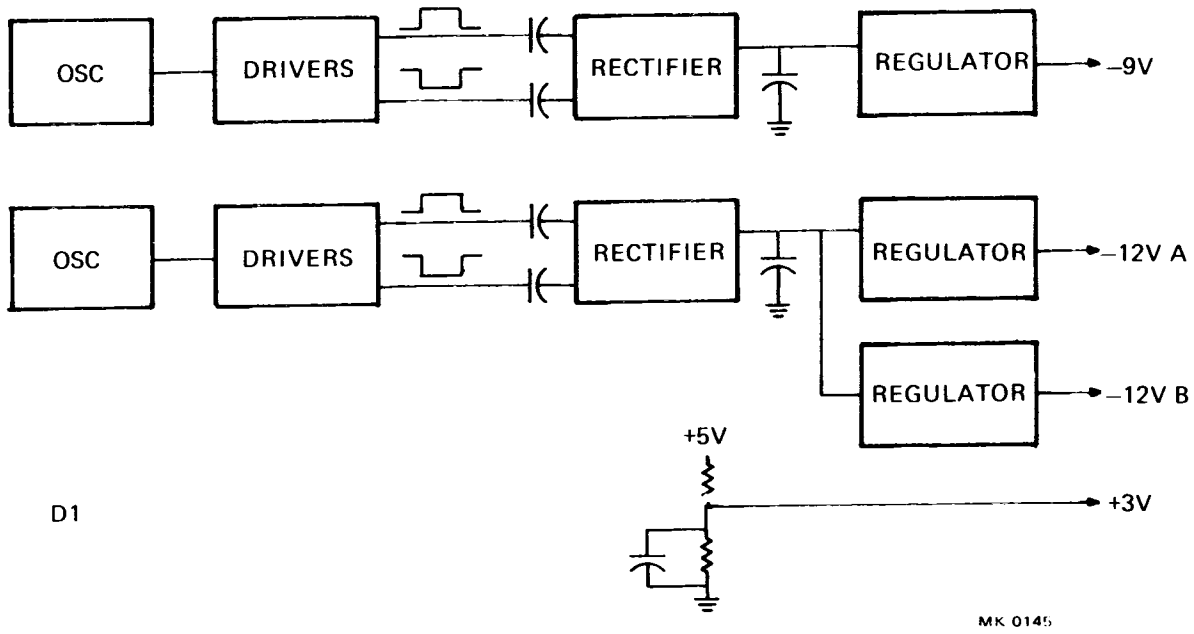


Figure 5-27 Power Supplies

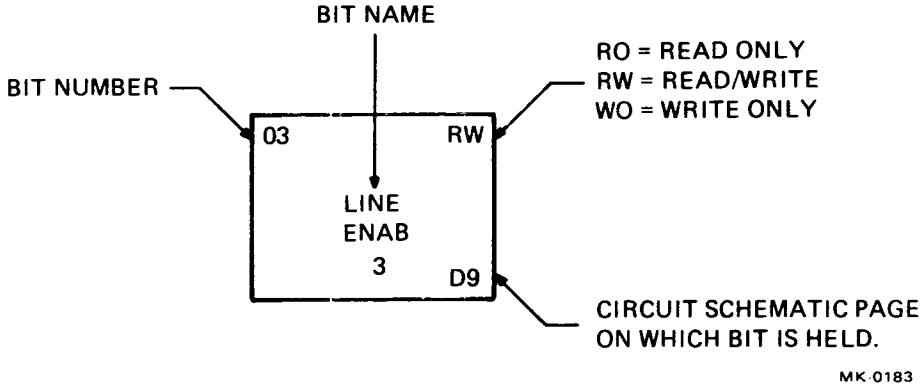


Figure 5-28 Bit Labeling Scheme

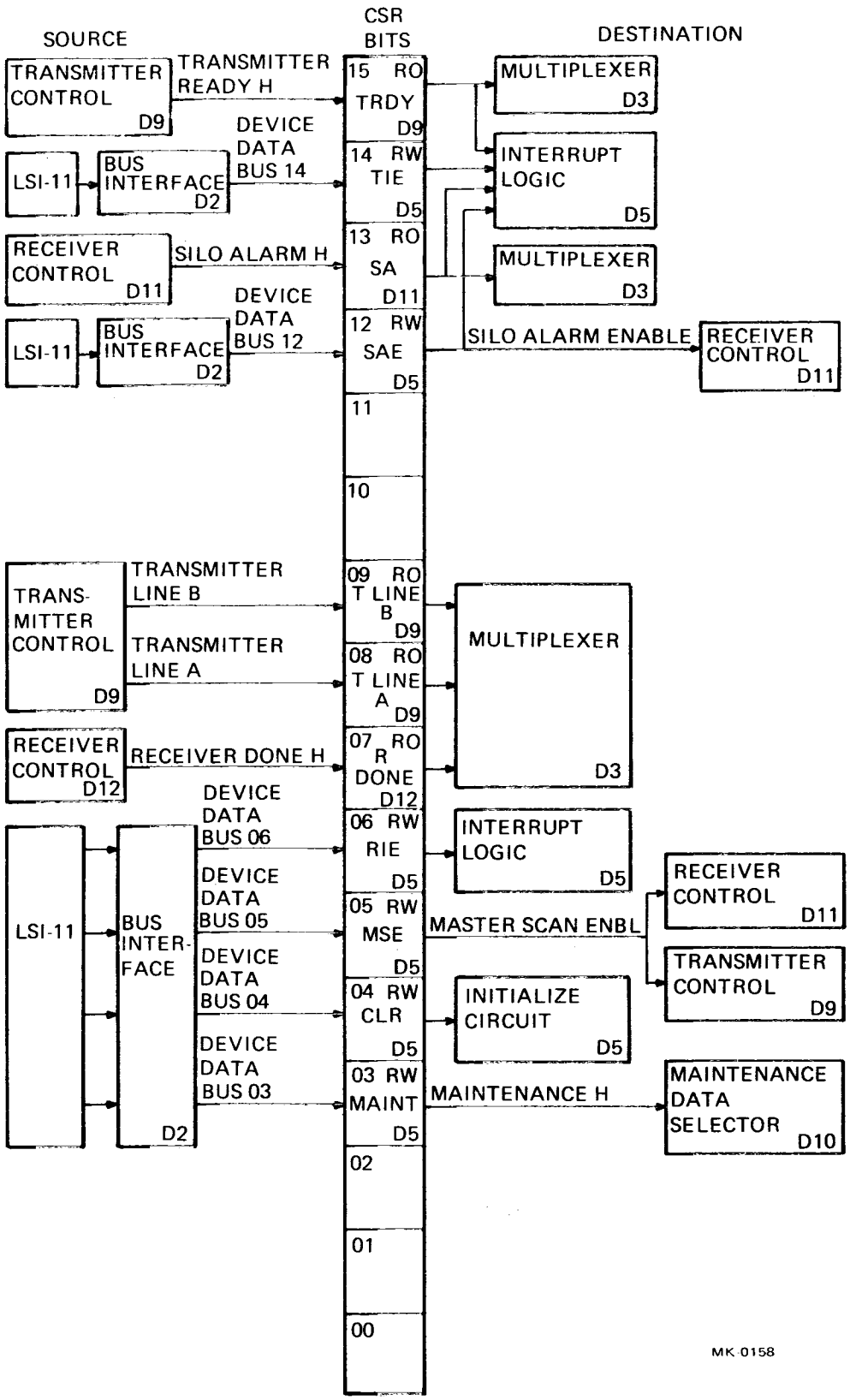


Figure 5-29 Control and Status Register

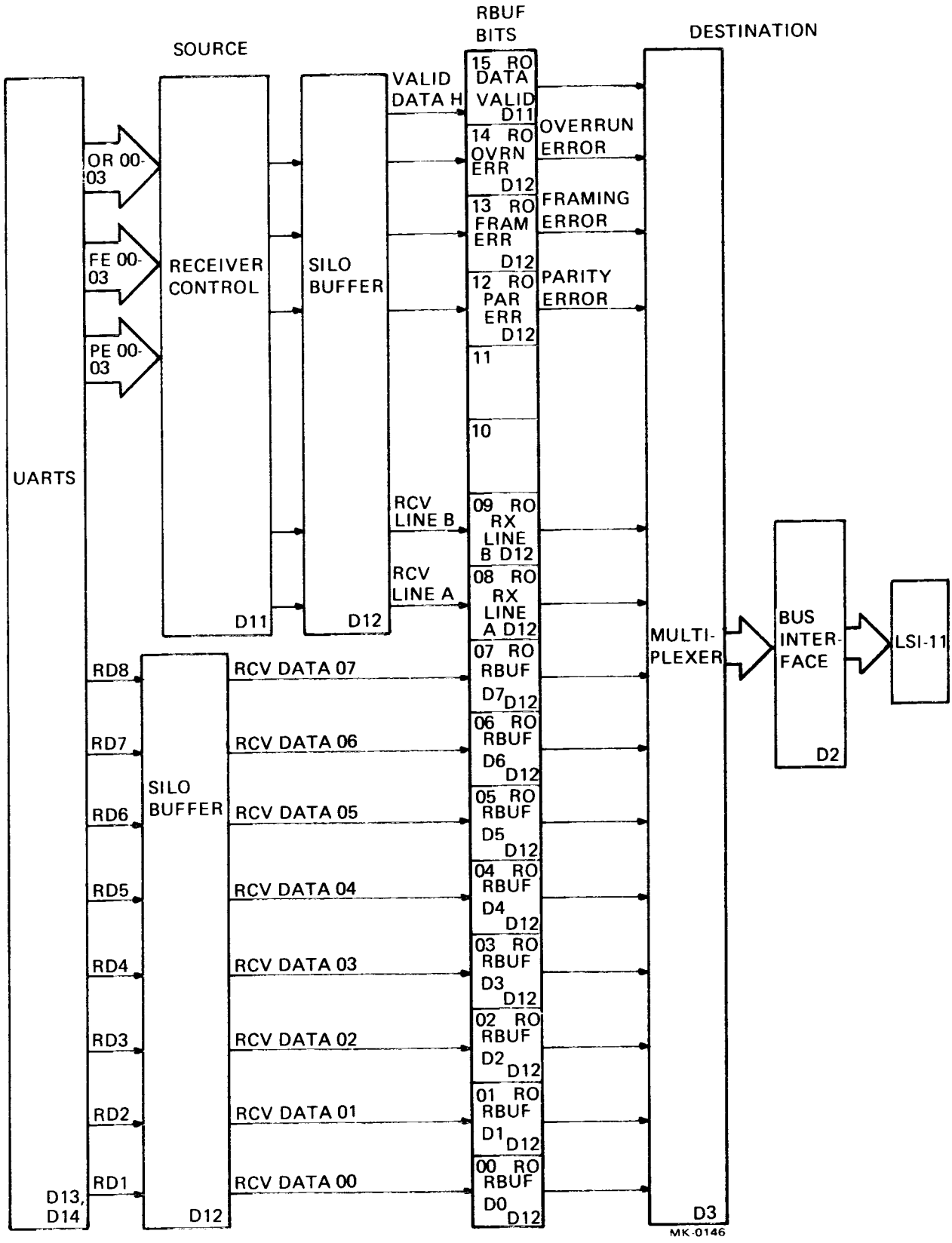


Figure 5-30 Receiver Buffer Register

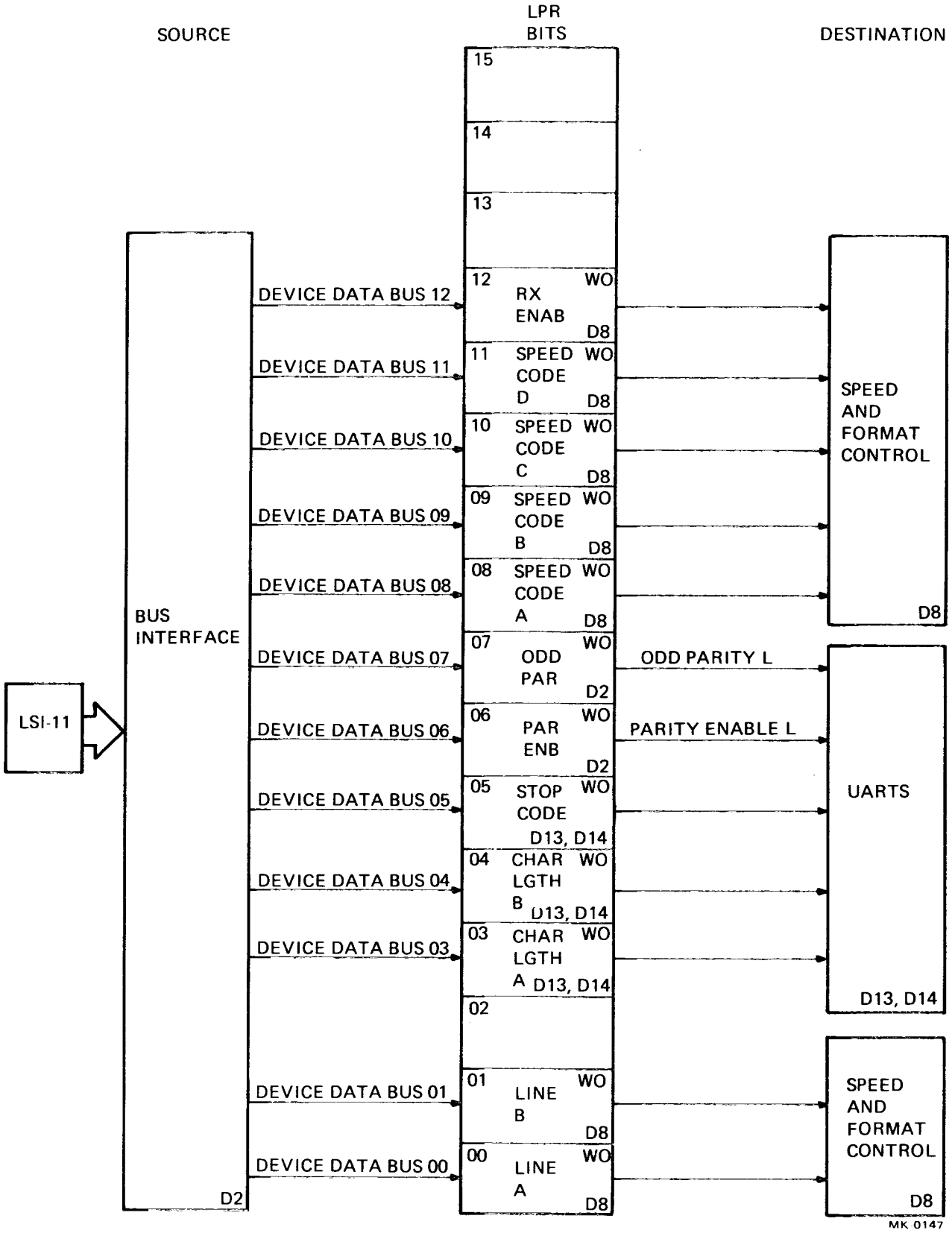


Figure 5-31 Line Parameter Register

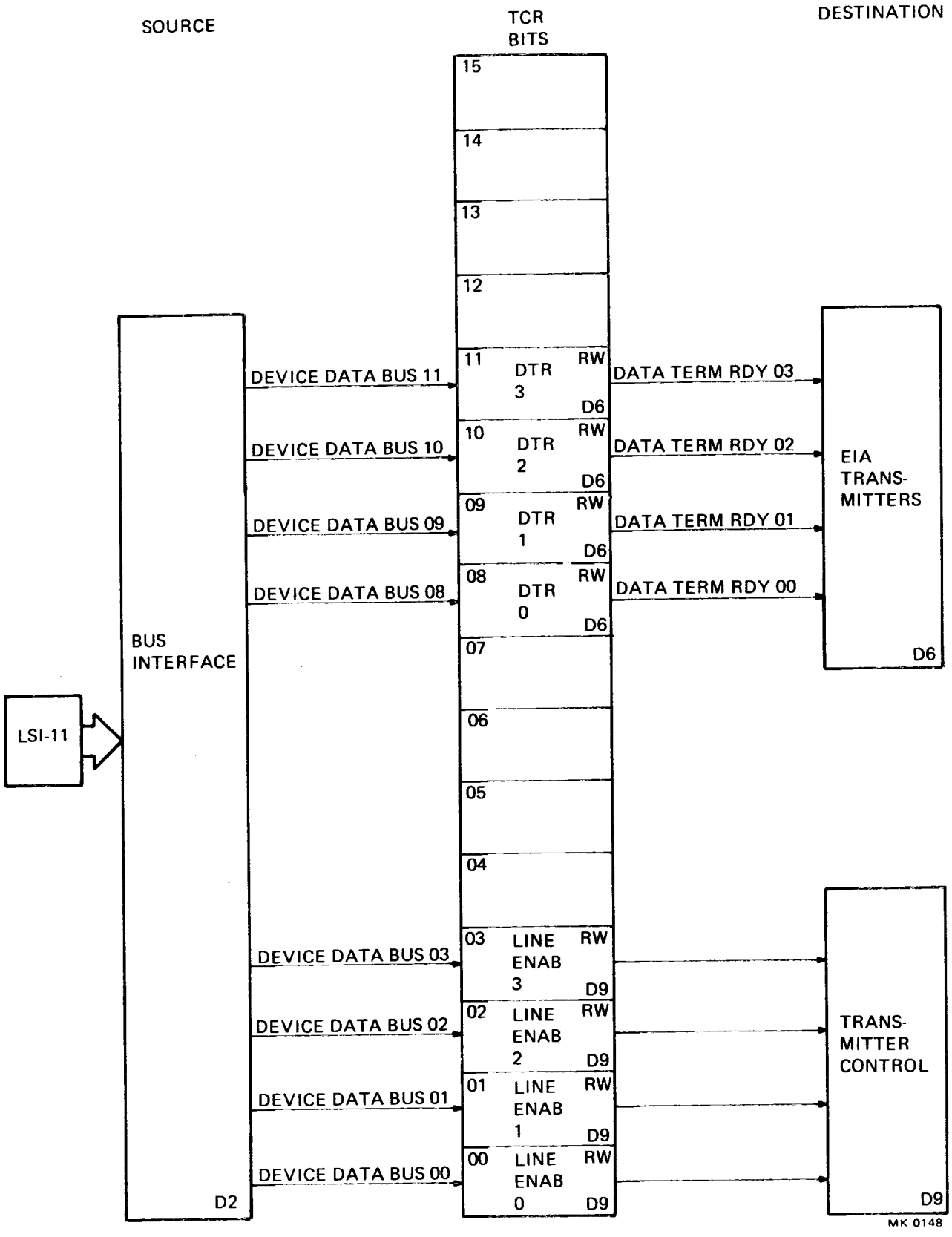


Figure 5-32 Transmit Control Register

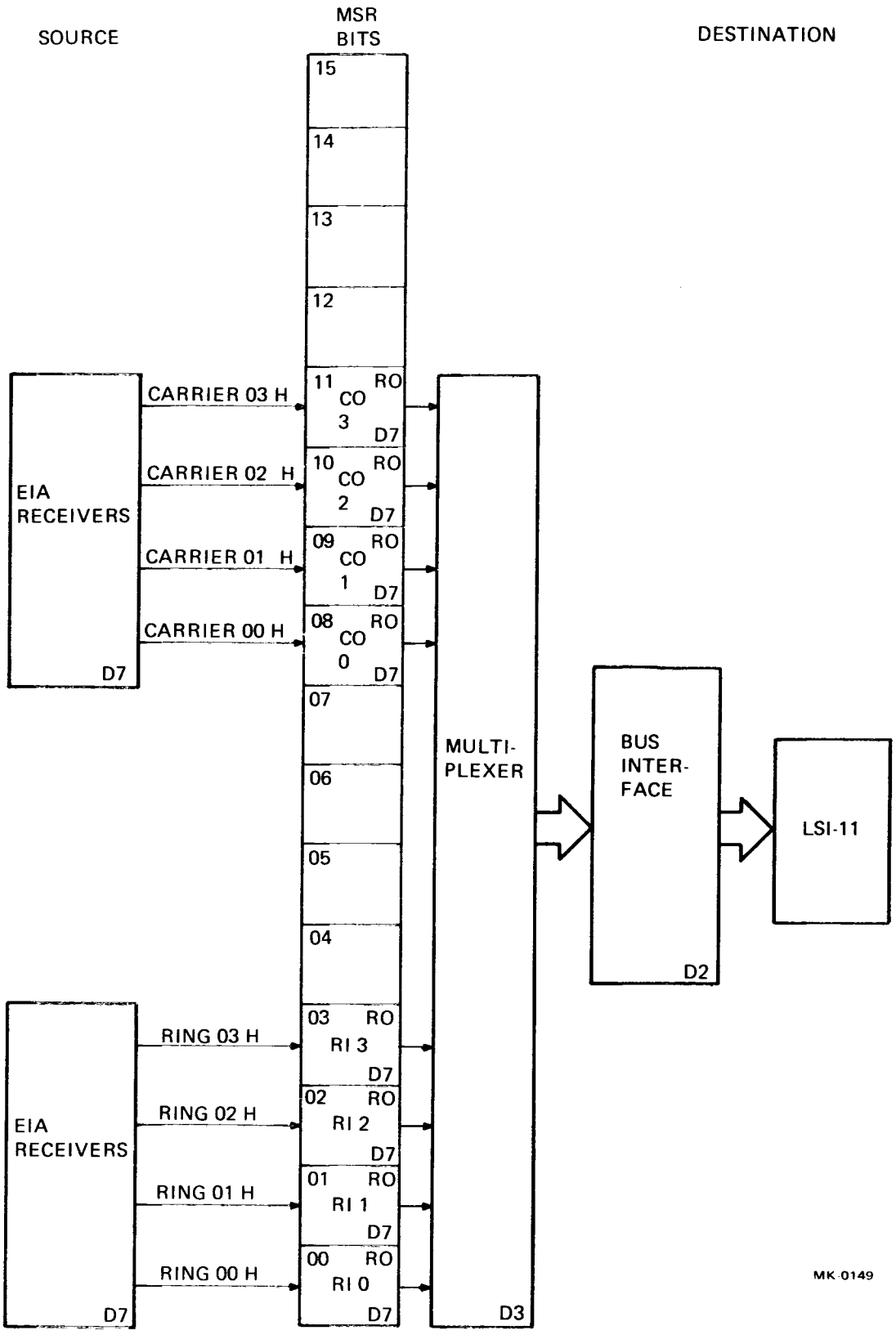


Figure 5-33 Modem Status Register

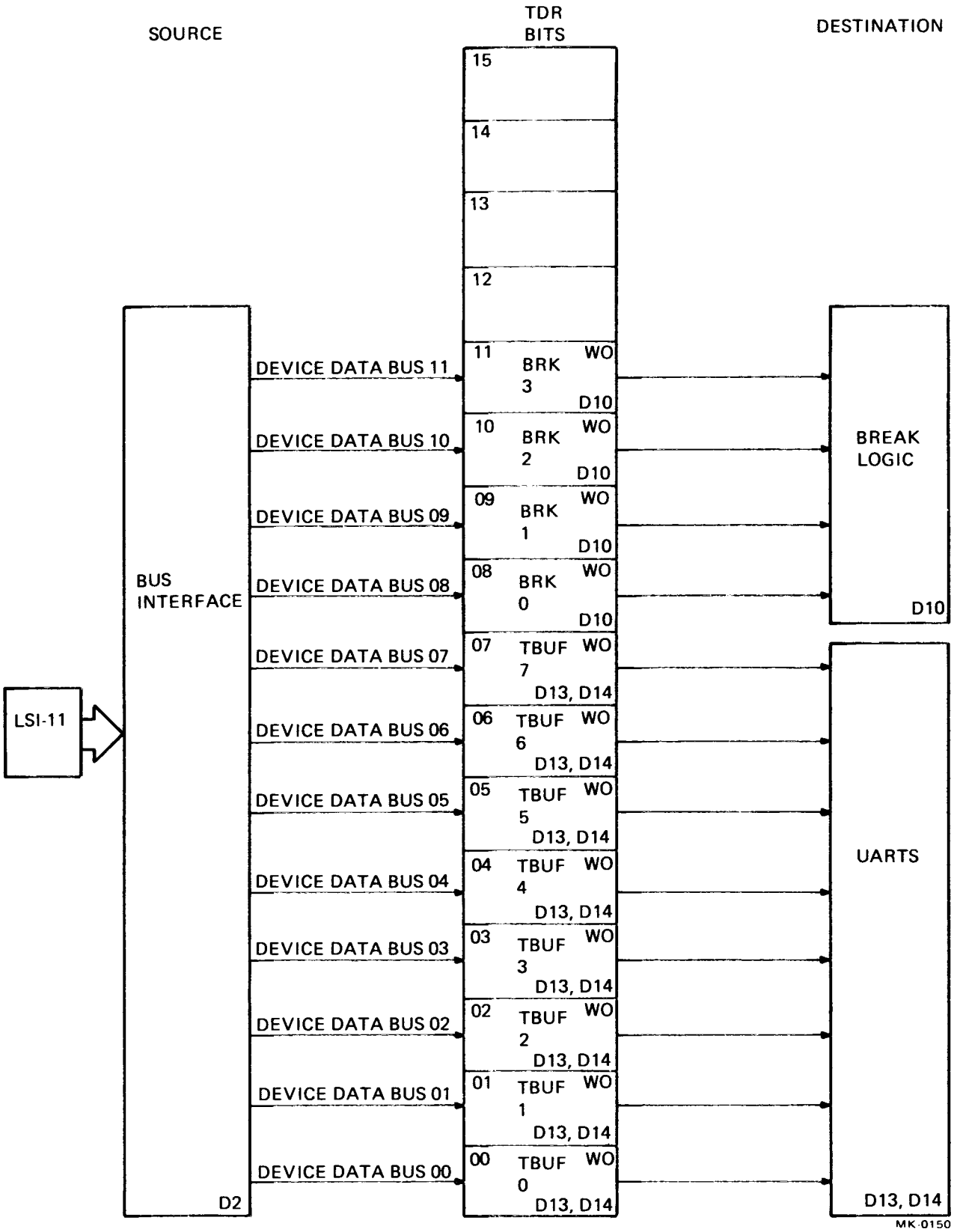


Figure 5-34 Transmit Data Register

CHAPTER 6
MAINTENANCE

6.1 SCOPE

The DZV11 is maintained by periodically exercising its functions to verify operation, and by replacing it with another module if it fails. Module-level repair is to be performed with automated test equipment at DIGITAL's repair centers. This chapter focuses on defining the existence of a DZV11 malfunction. If a malfunction is detected, the failing module should be tagged and turned in to the Logistics Group at the nearest DIGITAL Field Service Branch Office.

6.2 PREVENTIVE MAINTENANCE

There are no adjustments or other special requirements for the DZV11. Preventive maintenance consists of checking power supply voltages and running the exerciser program. This occurs as part of normal system maintenance. Similarly, the DZV11 option should be included in any cleaning and inspection effort performed on a system operating in a harsh or dirty environment. In summary, the preventive maintenance for the DZV11 is accomplished by normal system-level preventive maintenance.

6.3 CORRECTIVE MAINTENANCE

6.3.1 General

The need for corrective maintenance may be recognized by a failure during normal operation or by errors detected during system maintenance. Ideally, the DEC/X11 system exerciser program (MAINDEC-11-DXQLO) will indicate a failure by errors in one of its software modules. Once an error is detected (by either the operating system or the exerciser), the diagnostic programs are run to further isolate the failure. If the failure is isolated to a DZV11, the module is replaced. Refer to Chapter 2 for installation information.

This chapter gives a brief description of the diagnostic programs and test modes. For details refer to the program listings.

If it should become necessary to troubleshoot the DZV11 to the component-part level, consult the program listing on the use of looping features. By using the program to keep the option in the failing mode, and by using Chapter 5 and the circuit schematics to locate the related circuitry, a person may be able to isolate the problem to a failing component. This type of maintenance is not recommended if module replacement is possible.

6.3.2 Tools, Test Equipment, and Troubleshooting Aids

The minimum requirements for corrective maintenance are the programs listed in Table 6-1 and, if required by the system hardware configuration, a screwdriver to remove cover panels. The first two programs can test the DZV11 using the internal wrap-around feature described in Paragraph 5.4.11.

Table 6-1 Diagnostic Programs

Program Code	Program Title
MAINDEC-11-DVDZA	DZV11 ASYNC MUX PRT 1 OF 2
MAINDEC-11-DVDZB	DZV11 ASYNC MUX PRT 2 OF 2
MAINDEC-11-DVDZC	DZV11 CABLE & ECHO TST
MAINDEC-11-DVDZD	DZV11 OVERLAY FOR ITEP
MAINDEC-11-DZITA	INTERPROCESSOR TEST PROGRAM (ITEP)

More thorough checks can be made by using the H329 and H325 test connectors. The H329 connects data lines and control signals in a staggered loop-back configuration. This connector plugs into the Berg header connector on the module, and allows the diagnostic program to check out the entire board. The H325 test connector plugs into the modem end of the interface cable. It loops back data lines and control signals without staggering the lines. This allows the program to test both the module and the cable. These text connectors are illustrated in Figure 1-4 and their part numbers appear in Table 2-1.

If it is necessary to troubleshoot to the component-part level, an ohmmeter, an oscilloscope, and a quad extender card are also necessary. Before probing the module, make a thorough visual inspection for damaged parts or printed circuits.

6.3.3 DEC/X11 Exerciser Program

The DEC/X11 system run-time exerciser consists of various software modules configured to run interactively. The exerciser is unique to the system it exercises, and must be reconfigured if options are added to the system. Unlike the diagnostic programs, which thoroughly test the option in isolation, the exerciser tests the option's ability to run in the system environment. It does this by performing a representative sample of the option's functions while also testing other system components.

DZV11s that are shipped as part of systems are already included in the system exerciser. Those shipped as separate orders are not covered by the system exerciser, and DEC/X11 must be reconfigured to accommodate them. To build DEC/X11, refer to the *DEC/X11 User's Documentation and Reference Guide* (DEC part number MAINDEC-11-DXQBA).

The DZV11 module of DEC/X11 is titled, "DZBA DEC/X11 DZV11 ASYNCHRONOUS MODULE TEST" and is found in the DXQLO library (DEC/X11 LSI OPTIONS LIBRARY No. 1).

6.3.4 XXDP Diagnostic Programs

6.3.4.1 General– The diagnostic package consists of three stand-alone programs (DVDZA, DVDZB, and DVDZC) and an overlay for the interprocessor test program (DVDZD). To run the interprocessor test, it is necessary to first load the ITEP monitor (DZITA). These programs are available on the media listed in Table 6-2. Details of the programs may be found in the program listings. This paragraph presents general procedures and information.

Table 6-2 Multimedia Assignments

Media	Title	Part Number
Paper Tape	DZV11 DOC/PT KIT	ZJ251-RB
Floppy Diskette	RXDP #43 LSI #4	AS-C638n*-MC
Disk Packs		
(RK05)	CZZZCnn XXDP DIAG PKG3	AN-9695n-MC
(RK05)	CVZZDnn LSI-11 RKDP1 DIAG PKG	AN-9696n-MC
(RK06)	CZZRAnn RMDP DIAG PKG	AM-C751n-MC

*The n in the titles and part numbers indicates the revision level, and is subject to updating. For example, CZZZCV0 indicates Rev. V, patch 0 of CZZZC. Similarly, AN-9695V-MC indicates Rev. V in the part number.

6.3.4.2 Maintenance Modes – Figure 6-1 illustrates the data paths for the maintenance modes. The two basic programs (DVDZA and DVDZB) can be run in the internal, staggered, or external modes. The cable and echo test (DVDZC) can be selected either to loop characters from the program out through the test connector and back to the program, or else to loop characters from a test console through the DZV11 and back out to the test terminal. The interprocessor test program requires that another CPU be running the test along with the LSI-11 under test. The other CPU may be a local system, or a remote system (such as the turnaround system at DIGITAL in Maynard, Massachusetts). Refer to Figure 6-2. In this test, the two processors communicate to check the hardware from end to end. It is possible, however, to operate the program with an H325 loopback connector instead of another processor.

6.3.4.3 Setup Procedures – Running the internal loopback test requires no setup. The loopback function is enabled by CSR bit 03. The staggered loopback test requires that the module header connector be removed and replaced by a H329 test connector. The preferred method of doing this is to power down the computer, unplug the DZV11 module, and switch from the interface cable to the H329 test connector. The module is then reinstalled, taking care not to snag the components on anything, and the computer is powered up.

The external test requires that the far end of the BC11U interface cable be disconnected from the modem or terminal. Plug the H325 test connector into the modem-end of the cable.

Setup for the cable test also requires an H325, as indicated in Figure 6-1. The echo test requires a terminal connected to the DZV11. This may require a null modem, depending on the type of terminal.

Setup for the interprocessor test varies depending on the equipment available.

6.3.4.4 Software Switch Register – The LSI-11 uses location 176 for a switch register instead of front panel swtiches. To change the operating parameters, load the program and then use the ODT slash command to open location 176. Refer to the applicable program listing for a definition of bits. Assemble the corresponding octal number and enter it into location 176. Then start the program at location 200.

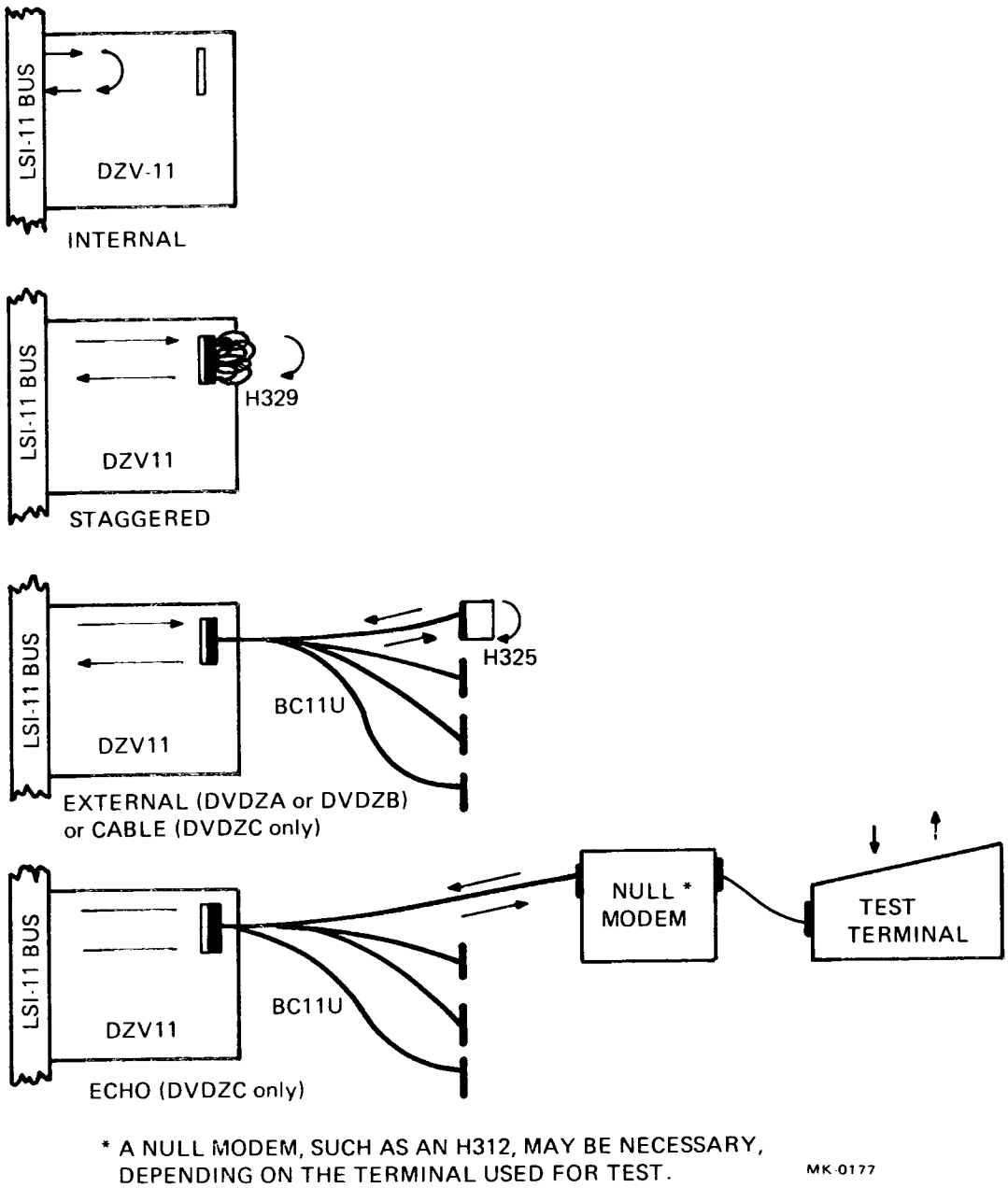


Figure 6-1 Maintenance Mode Data Flow

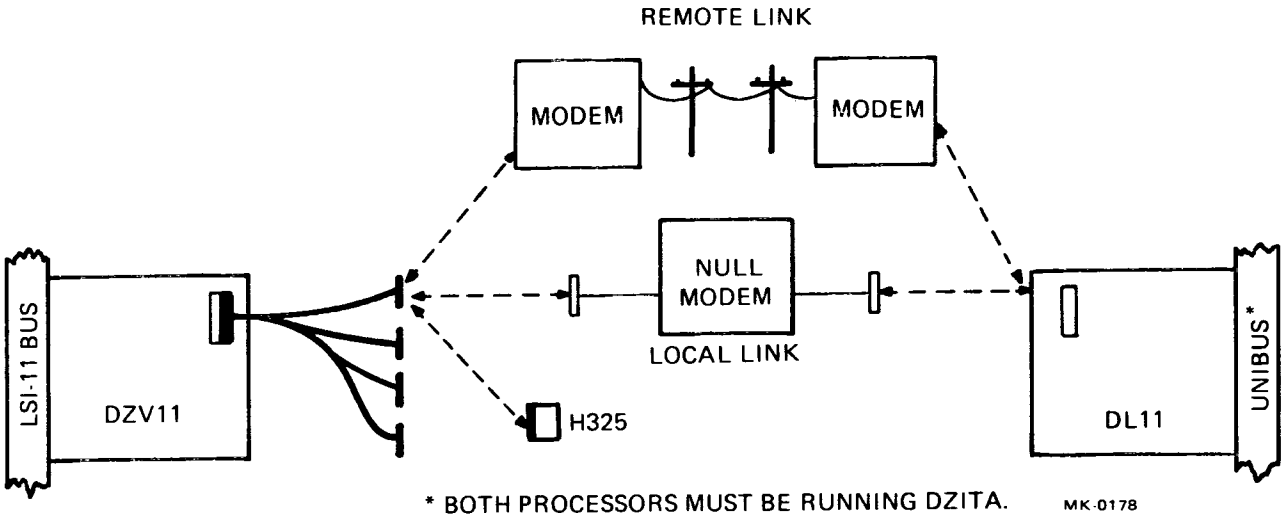


Figure 6-2 Interprocessor Test (ITEP)

The software switch register may be accessed while the program is running. Type a CONTROL G to stop the program and open the switch register.

6.3.4.5 Auto-Sizing – The two basic tests (DVDZA and DVDZB) have auto-sizing capabilities, and may therefore be run without modification of the switch register.

The auto-sizer routine detects all DZV11 device and vector addresses within the floating address and vector area. The values of the other parameters are by default set for 19.2K baud, internal loopback, and the testing of all four lines. These values are stored in a status table in locations 1500 through 1740 (Table 6-3). They are printed by the console terminal during the test.

6.3.4.6 Parameter Inputs and Dialogue – The DVDZA and DVDZB diagnostics may be run with parameters specified by the operator. To do this, set bit 00 in the software switch register and then start the program at location 200. The program responds with a series of questions.

1st CSR ADDRESS (160000:163770):

Answer this question by typing in the address of the DZV11 CSR at which you wish testing to begin. Follow all answers with a carriage return.

1st VECTOR ADDRESS (300:770):

Type the vector of the DZV11. Note that all the DZV11s must be contiguous for both address and vector locations.

Table 6-3 Typical Map of DZV11 Status*

Location	Contents	Meaning
1500	160100	CSR address of first DZV11 in system.
1502	000300	Receiver interrupt vector for first DZV11 in system.
1504	000017	TCR bit representation of active lines to be tested.
1506	017470	LPR bits representing the following: receiver enabled, 19.2K baud, 8 bits per character, and 2 stop bits.
1510	000000	Indicates the selected maintenance mode, where: 000000 = Internal 000200 = External with H325 100000 = Staggered with H329

*This table is an example. Consult the program listing for details.

```
MAINTENANCE MODE
    (EXTERNAL (H325) (E))
    (INTERNAL (DZCSR03=1) (I))
    (STAGGERED (H329) (S))
```

Type an E, I, or S, as appropriate. If running external, all selected lines must be terminated by H325 test connectors.

```
# OF DZV11s (IN OCTAL) (1:20):
```

Type the total number of DZV11s to be tested.

Other parameters (e.g., baud rate) that are not included in the opening dialogue may be entered via the software switch register. All extra parameters are assigned to all DZV11s in the system. The program run time is approximately 1.5 minutes on the first pass and 2.5 minutes on subsequent passes. Run at least three error-free passes.

Operation of the cable and echo test (DVDZC) always requires an opening dialogue. Special switch settings, however, are not required for normal operation. Start the program and respond to the questions with an answer followed by a carriage return

```
VECTOR ADDRESS -
```

Type the vector of the DZV11 under test.

CONTROL REGISTER ADDRESS -

Type the CSR address of the DZV11 under test.

WHICH TEST? ECHO OR CABLE (E OR C)

Type E or C, as required.

BAUD RATE -

Type one of the following: 50, 75, 110, 135, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, or 9600.

LINE -

Type the number of the line that has the H325 test connector on it. The lines are numbered 0, 1, 2, 3.

At this point, the test begins.

Cable Test
If the cable test (C) was selected, the system prints:

CABLE TEST

The cable text executes in approximately 15 seconds at 9600 baud. It prints an end-of-pass message after each pass. To change lines, strike any key on the console terminal while the program is running. The system responds with:

LINE:

At this point, change the H325 test connector to another line and type the new line number. The system prints:

CABLE TEST

and continues.

Echo Test
If the echo test (E) is selected when the program asks which test, the subsequent baud rate and line questions are answered the same way. After the line number is typed, the system prints:

TERMINAL ECHO TEST

on the console terminal, and prints:

THE QUICK BROWN FOX JUMPED OVER THE LAZY DOGS BACK 0123456789

on the DZV11 terminal. To have this message printed continuously, type a CONTROL G on the console terminal while the message is being printed by the DZV11 terminal. The program prints a prompt character on the console terminal and waits for a new switch register setting. Set the switch register to 377 to have the program output on the quick brown fox message continuously.

To return to the normal flow of the diagnostic, type a CONTROL G and change the switch register to something other than 377.

The console terminal prints:

TYPE A CHAR. ON DZV11 TERMINAL

At this point, any printable character typed on the DZV11 terminal is echoed back to that terminal.

If a CONTROL C is typed on the DZV11 terminal, the program prints the end-of-pass message on the console and then resumes with the quick brown fox message on the DZV11 terminal.

To change lines, type any printable character on the console terminal. The system prints:

LINE:

and waits for a response. Plug the next line into the DZV11 terminal and continue until all the lines have been tested. Refer to the listing for explanations of error printouts.

6.3.4.7 Functional Description – This paragraph briefly describes the diagnostic programs used with the DZV11. For a more detailed treatment, refer to the program listings.

DVDZA – This is the first of a 2-part series used for basic option checkout. It exercises the read/write bits of the registers, performs simple transmission and reception exercises for each line, and verifies the interrupt capabilities of the option (Table 6-4).

Table 6-4 DVDZA Tests

Test Number	Functions
1	Proves the bus reply response during a read or write to the following device registers: CSR, RBUF, TCR, and MSR.
2	Proves that bit CLR can be set, and that it will clear by itself.
3	Verifies that the read/write bits of the CSR can be set. Then verifies that they can be cleared. Also verifies that after being set again, they can be cleared by a Master Clear. The bits tested are: MAINT, MSE, SAE, RIE, and TIE.
4	Tests that all of the TCR bits can be set, cleared, and cleared by a Master Clear. Also tests that the DTR bits can be set, cleared, and cleared by a RESET.
5	Verifies that RDONE, TRDY, TLINE B, TLINE A, and SA are read-only. Tests that TRDY is zero until a line is selected and MSE is set.
6	Tests that the following CSR bits are read-write: TIE, SAE, MSE, and MAINT. Checks that setting CLR in the CSR will clear these bits.
7	Performs reset testing. Also tests read-only bits in RBUF and write-only bits in LPR.

Table 6-4 DVDZA Tests (Cont)

Test Number	Functions
10	Performs reset testing. Also tests read-only bits in the MSR and write-only bits in the TDR.
11	Verifies that setting DTR causes CO and RI to set under the following circumstances: 1. For the same line if in external mode 2. For the staggered line if in staggered mode. Lines are staggered as follows: line 0 with line 1, line 2 with line 3. This test is run only if an H325 or H329 is connected to the DZV11 under test.
12	Verifies that TRDY is set when a line is ready to be loaded. Verifies that the line specified by TLINE A and TLINE B in the CSR corresponds to the line selected in the TCR.
13	Transmits one character and receives one character on one line at a time. The character is 252. All selected lines will be turned on. This is the first time any data is checked in the receiver. Using switch 09 with this test establishes a tight scope loop that transmits a steady stream of characters.
14	Clears RX ENAB in the LPR for each line to verify that each receiving line can be disabled. This test also verifies that the silo can be emptied by setting CLR in the CSR.
15	Proves that the transmitter transmits characters and the receiver receives characters. One line at a time is tested, based upon valid lines. This is the first point at which all data is tested.
16	Exercises one line at a time to prove that: 1. The transmitter BRK bit works. 2. The receiver can flag framing errors. 3. The receiver can flag parity errors.
17.	Verifies that the DZV11 does not interrupt while the processor status does not allow interrupts. Also checks that the DZV11 can interrupt when the processor status does allow interrupts.
20	Verifies that the receiver interrupts before the transmitter, even when the transmitter was enabled first.

DVDZB – This program is the second of the two basic option diagnostics. It exercises the transmitters and receivers in all possible operating modes and at all possible data rates. Error conditions are induced and the option is checked for the ability to recognize these errors (Table 6-5).

Table 6-5 DVDZB Tests

Test Number	Functions
1	Verifies OVRN ERR and SA one line at a time, based upon valid lines. As each of the first 16 characters are sent, Silo Alarm is tested to be cleared. On the 16th character, the program tests for Silo Alarm to set. Then the entire silo is filled and an overrrun error is expected on the 65th character. Using switch 09 for this test sends 20 characters on the line previously selected. This occurs continuously while SW09 = 1.
2	Tests that SAE inhibits interrupts. Sets RIE and checks that SA causes an interrupt on the 16th character. Tests all selected lines one at a time.
3	Interrupt test on the transmitter and receiver. Runs all qualified lines at maximum speed.
4	DZV11 relative timing test. Each selected line, one at a time, runs 16 characters at all baud rates, and then the highest baud rate with all character lengths. Each successive parameter decreases in time from the previously selected parameter. The time is checked aginst the previous time. The parameters are: 1. Eight bits per character plus two stop bits at 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, and 9600 baud. 2. Five, six, and seven bits per character with two stop bits and at 19.2K baud. Each line completes all of the checks before the next line is tested.
5	Checks parity errors in staggered mode only. All selected lines are enabled simultaneously. Tests for even parity on odd lines and odd parity on even lines. Then it checks the reverse. The test verifies that PAR ERR can be set.

DVDZC – This program verifies the cable interface connection between the module and the EIA connector. The diagnostic includes a cable test, an echo test, and a test of modem control signals.

The cable test transmits a binary count pattern via the test connector to the receivers. The data flow is from the program out through the interface cable to the test connector, and back.

The echo test accepts one character at a time and retransmits that character on the same line. The data flow is from a test terminal in through the interface cable and DZV11 to the program and back out to the terminal.

The third test verifies that setting DTR for a given line causes CO and RI to set. Jumpers W1, W2, W3, and W4 must be installed for this test.

6.3.5 Interprocessor Test (ITEP)

The interprocessor test program (ITEP) verifies the operation of the DZV11 by using it in a communications link with another processor. The other processor may be on an LSI-11 or PDP-11 system at the same location as the system under test, or it may be in a remote communications test center. DVDZD is the DZV11 overlay of the test program. It must be run along with DZITA-D, the monitor program.

ITEP has four testing modes. The overlay performs the following functions in the four modes.

Internal Loopback Mode

1. Establishes the modem connection.
2. Waits to receive a message terminated by the receive terminating character (001).
3. Verifies the data against the data selected by SW09 and SW10 (SW07 = 0).
4. Transmits the data selected by SW09 and SW10 (SW08 = 0), or transmits the received data (SW08 = 1).
5. Returns to monitor for "END PASS" (SW04 = 1), or goes to step 1 (SW04 = 0).

External Loopback Mode (Full-Duplex Only)

1. The overlay establishes the modem connection.
2. Transmits the selected data.
3. Enables the receiver.
4. Waits for the message to be received.
5. Verifies the data (SW07 = 0).
6. Returns to the monitor for "END PASS" (SW04 = 1) or goes to step 1 (SW04 = 0).

One-Way-In Mode

1. The overlay establishes the modem connection.
2. Enables the receiver.
3. Waits for the message to be received.
4. Verifies the data (SW07 = 0).
5. Returns to the monitor for "END PASS" (SW04 = 1) or goes to step 1 (SW04 = 0).

One-Way-Out Mode

1. The overlay establishes the modem connection.
2. Enables the transmitter.
3. Transmits the selected data.
4. Returns to monitor for "END PASS" (SW04 = 1) or goes to step 1 (SW04 = 0).

6.3.5.1 Starting ITEP– ITEP requires a complete communications loop (Figure 6-2). Ensure that a loop is established with compatible equipment. The variable parameters must be the same in each of the two processors. The mode must be one of the options listed in Table 6-6. The system that is to receive data first should be loaded and started first. If the modem being used on this system has an automatic answer feature, it should be enabled. The system that is to transmit first should then be loaded and the connection established. If the LSI-11 line clock is to be used, it should be enabled prior to program execution. The load address is 200. Refer to the program listing for details regarding restrictions, error messages, and optional selections.

Table 6-6 Valid Mode Combinations

CPU No. 1	CPU No. 2
One-Way-Out	One-Way-In
One-Way-In	One-Way-Out
External Loopback	Internal Loopback
Internal Loopback	External Loopback
External Loopback (full-duplex)	External Loopback (full-duplex)
External Loopback (full-duplex with H325 test connector on end of modem cable)	

6.3.5.2 Console Dialogue– After the program has been started, the dialogue for input parameters proceeds as follows.

1. The program types the name of the overlay, followed by a question mark. If you wish to set up just the indicated overlay, type a carriage return.

2. The program types the default address of 160010. Type a carriage return if the default address is correct for the DZV11. If not, type the actual CSR address.

3. The program types the default vector address of 300 and a question mark. Type a carriage return to use the defult vector. If using a different vector, type the actual vector.

4. The program types 200 as the priority setting. For the LSI-11, this indicates that the processor will acknowledge interrupts. For a PDP-11, this indicates priority level 4. Type a carriage return to use this priority. If a different priority is required on a PDP-11, type the appropriate code (240 for priority level 5, 300 for priority level 6, etc.).

5. Next the program types the default value for parameter no. 1 of 011070 and a question mark. Type a carriage return to use the default value. To select a different value, refer to Tables 6-7 and 6-8.

NOTE

If any of the values in items 2 through 5 are changed, the new value becomes the default value for subsequent restarts of the program.

Table 6-7 Meaning of Parameter No. 1

Bits 0, 1	Line number being used; default setting is for line 0.
Bits 3, 4	Character length; default is 8 bits.
Bit 5	Stop bit count; default is 2 stop bits.
Bits 6, 7	Parity enable and select; default is no parity.
Bits 8–11	Baud rate select; default is 110 baud.
Bit 12	Receiver on (this should always be set).

Table 6-8 Parameter No. 1 Examples

Value*	Baud Rate
10070	50
10470	75
11070	110
11470	134.5
12070	150
12470	300
13070	600
13470	1200
14070	1800
14470	2000
15070	2400
15470	3600
16070	4800
16470	7200
17070	9600

*These examples set the receiver for line 0, set the baud rate as listed, and set the format for 8 bits per character with 2 stop bits and no parity. For definitions of the other possible settings, refer to Table 3-4.

6.3.5.3 Operational Switch Settings – The program instructs the operator to set console switches. On a PDP-11 with front panel switches, set the switches according to Table 6-9. On an LSI-11, modify the contents of the software switch register (location 176) according to Table 6-9. If no change is desired, type a carriage return. If an error is made while modifying the software switch register, CONTROL U allows re-entering the correct value. The contents of the switch register can be changed during program run time by typing a CONTROL G and then entering a new value.

Table 6-9 Operational Switch Settings

SW15 = 1	Halt on error
SW14 = 1	Single pass SW14 has no effect if SW04 = 0.
SW13 = 1	Inhibit error typeouts
SW12 = 1	Inhibit all typeouts except errors. If SW12 = 0 and SW04 = 1, END PASS is typed and transmitted/received data is typed.
SW11 = 1	Use previously specified data.
SW10 = 1	Data select (with SW09)
SW09 = 1	Data select (with SW10) 00 = 1 Get data from operator. 01 = 1 Test message no.1 ($A quick brown fox) 10 = 1 Test message no.2 ($B numerics) 11 = 1 Test message no.3 ($C comtest/quick brown fox/numerics)
SW08 = 1	Transmit received data (internal loopback mode).
SW07 = 1	Do not test received data.
SW06 = 1	Monitor transmitted data on console terminal.*
SW05 = 1	Monitor received data on console terminal.*
SW04 = 1	Return to monitor for END PASS. When SW04 = 0, program loops in the overlay, never returning to the monitor.
SW03 = 1	Internal loopback mode
SW02 = 1	External loopback mode
SW01 = 1	One-way-in mode
SW00 = 1	One-way-out mode

*In many cases, not all the data appears on the console terminal. This is especially true when the communications interface is running at a faster baud rate than the console, but even at equal or slower baud rates, not all characters may appear on the console.

When the communication link is established and the dialogue has been completed, start the program by using the CONTINUE switch (on a PDP-11) or the ODT P command (on an LSI-11).

6.3.5.4 Testing – If one-way-in or internal loopback modes are selected, the program sets Data Terminal Ready and waits for data. If one-way-out or external loopback modes are selected, the program sets Data Terminal Ready and then waits for the Carrier bit before attempting to transmit data.

NOTE

For example, to test a line in external loopback mode with message no. 3, use a switch setting of 3024.

6.3.6 Manual Tests

This paragraph contains several short tests that can be performed using the hardware ODT commands. The examples given here assume that the reader is familiar with the use of ODT and that the DZV11 CSR address is set for 160010. The letter n is used to indicate a number that may vary. For an explanation of ODT commands, refer to *1977–78 Microcomputer Handbook*, Section 2, Chapter 2.

1. This test verifies that the CLR bit will clear the CSR and the low byte of the TCR.

@160010/000000 <LF>	Open the CSR
160012/0nnnnn <LF>	Open the RBUF.
160014/000000 <LF>	Open the TCR.
160016/000000 <CR>	Open the TDR.
@160010/000000 10050 <LF>	Open CSR; enter bits.
160012/0nnnnn <LF>	
160014/000000 7417 <LF>	Open TCR; enter bits.
160016/000000 <CR>	
@160010/111450 20 <LF>	Open CSR; set device clear.
160012/0nnnnn <LF>	
160014/007400 <LF>	Observe that low byte of TCR is cleared.
160016/000000 <CR>	The MSR may contain a value of 007417 if the H329 is connected.
@160010/000000	Observe that CSR is cleared.

2. This test makes a basic check of the transmitter scanner. It performs a Master Clear, sets the TCR bit for line 3, and then verifies that line 3 appears in the CSR. It clears the TCR bit for line 3 and then checks that the line numbers in the CSR are clear.

@160010/000000 20 <CR>	Set Master Clear.
@/000000 50 <LF>	Set MSE and MAINT.
160012/0nnnnn <LF>	
160014/000000 10 <↑>	Set TCR bit 03.
160012/0nnnnn <↑>	
160010/101450 <LF>	Read CSR for TRDY set and Tx line = 3.
160012/0nnnnn <LF>	
160014/000010 0 <↑>	Clear TCR bit 03.
160012/0nnnnn <↑>	
160010/000050	Read CSR for TRDY and TLINEs cleared.

To perform the same test on line 2, proceed as follows.

@160010/000000 20 <CR>	Set Master Clear.
@/000000 50 <LF>	Set MSE and MAINT in CSR.
160012/0nnnnn <LF>	
160014/000000 4 <↑>	Set TCR bit 02.
160012/0nnnnn <↑>	
160010/101050 <LF>	Check CSR for TRDY set and Tx line = 2.
160012/0nnnnn<LF>	
160014/000004 0 <↑>	Clear TCR bit 02.
160012/0nnnnn <↑>	
160010/000050	Check CSR for TRDY and TLINEs cleared.

To perform the same test on line 1, proceed as follows.

@160010/000000 20 <CR>	Set Master Clear.
@/000000 50 <LF>	Set MSE and MAINT in CSR.
160012/0nnnnn <LF>	
160014/000000 2 <↑>	Set TCR bit 01.
160012/0nnnnn <↑>	
160010/100450 <LF>	Check CSR for TRDY set and Tx line = 1.
160012/0nnnnn <LF>	
160014/000002 0 <↑>	Clear TCR bit 01.
160012/0nnnnn <↑>	
160010/000050	Check CSR for TRDY and TLINEs cleared.

To perform the same test on line 0, proceed as follows.

@160010/000000 20 <CR>	Set Master Clear.
@/000000 50 <LF>	set MSE and MAINT in CSR.
160012/0nnnnn <LF>	
160014/000000 1 <↑>	Set TCR bit 00.
160012/0nnnnn <↑>	
160010/100050 <LF>	Check CSR for TRDY set and Tx line = 0.
1600012/0nnnnn <LF>	
160014/000001 0 <↑>	Clear TCR bit 00.
160012/0nnnnn <↑>	
160010/000050	Check CSR for TRDY and TLINEs cleared.

3. This next test checks that line 3 is the highest priority line when all lines are enabled at once. It checks that line priority goes from 3 to 0.

@160010/000000 20 <CR>	Set Master Clear.
@/000000 50 <LF>	Set MSE and MAINT in CSR.
160012/0nnnnn <LF>	
160014/000000 17 <↑>	Set TCR bits for lines 3, 2, 1, and 0.
160012/0nnnnn <↑>	
160010/101450 <LF>	Check CSR for TRDY set and Tx line = 3 (highest priority line).
160012/0nnnnn <LF>	
160014/000017 7 <↑>	Clear only TCR bit 3.
160012/0nnnnn <↑>	
160010/101050 <LF>	Check CSR for TRDY set and Tx line = 2 (next highest priority).
160012/0nnnnn <LF>	
160014/000007 3<↑>	Clear TCR bit 02.
160012/0nnnnn <↑>	
160010/100450 <LF>	Check CSR for TRDY set and Tx line = 1 (third highest priority).
160012/0nnnnn <LF>	
160014/000003 1 <↑>	Clear TCR bit 01.
160012/0nnnnn<↑>	
160010/100050 <LF>	Check CSR for TRDY set and Tx line = 0 (lowest priority).
160012/0nnnnn <LF>	
160014/000001 0 <↑>	Clear TCR bit 00.
160012/0nnnnn <↑>	
160010/000050	Check CSR for TRDY and TLINEs cleared.

4. This test checks the receiver without using the transmitter scanner. The BRK bit is set and the RBUF is tested to see that it contains an all-zero character and a framing error.

@160010/000000 20 <CR>	Set Master Clear.
@/000000 50 <LF>	Set MSE and MAINT in CSR.
160012/0nnnnn 17470 <LF>	Load LPR with 19.2K baud, 8-level, 2 stop bits, and line 0.
160014/000000 <LF>	
160016/000000 400 <CR>	Set Break bit in TDR for line 0.
@160010/000250 <LF>	Read CSR for RDONE set.
160012/120000 <↑>	Check RBUF for Data Valid and FRAM ERR set, for RX line = 0, and for all zeros in data bits.
160010/000050 <LF>	Check CSR for RDONE cleared.
160012/020000	Check RBUF for Data Valid cleared.

To perform the same test on line 1, proceed as follows.

@160010/000000 20 <CR>	Set Master Clear.
@/000000 50 <LF>	Set MSE and MAINT in CSR.
160012/0nnnnn 17471 <LF>	Load LPR with 19.2K baud, 8-level, 2 stop bits, and line 1.
160014/000000 <LF>	
160016/000000 1000 <CR>	Set Break bit in TDR for line 1.
@160010/000250 <LF>	Check CSR for RDONE set.
160012/120400 <↑>	Check RBUF for Data Valid and FRAM ERR set, for RX line = 1, and for all zeros in data bits.
160010/000050 <LF>	Check CSR for RDONE cleared.
160012/020400	Check RBUF for Data Valid cleared.

To perform this test on line 2, proceed as follows.

@160010/000000 20 <CR>	Set Master Clear.
@/000000 50 <LF>	Set MSE and MAINT in CSR.
160012/0nnnnn 17472 <LF>	Load LPR with 19.2K baud, 8-level, 2 stop bits, and line 2.
160014/000000 <LF>	
160016/000000 2000 <CR>	Set Break bit in TDR for line 2.
@160010/000250 <LF>	Check CSR for RDONE set.
160012/121000 <↑>	Check RBUF for Data Valid and FRAM ERR set, for RX line = 2, and for all zeros in data bits.
160010/000050 <LF>	Check CSR for RDONE cleared.
160012/021000	Check RBUF for Data Valid cleared.

To perform this test on line 3, proceed as follows.

@160010/000000 20 <CR>	Set Master Clear.
@/000000 50 <LF>	Set MSE and MAINT in CSR.
160012/0nnnnn 17473	Load LPR with 19.2K baud, 8-level, 2 stop bits, and line 3.
160014/000000 <LF>	
160016/000000 4000 <CR>	Set Break bit in TDR for line 3.
@160010/000250 <LF>	Check CSR for RDONE set.
160012/121400 <↑>	Check RBUF for Data Valid and FRAM ERR set, for Rx line = 3, and for all zeros in data bits.
160010/000050 <LF>	Check CSR for RDONE cleared.
160012/021400	Check RBUF for Data Valid cleared.

5. This test transmits and receives several characters on line 0. It uses 8-level with 2 stop bits at 19.2K baud in maintenance mode.

@160010/000000 20 <CR>	Set Master Clear.
@/000000 50 <LF>	Set MSE and MAINT in CSR.
160012/0nnnnn 17470	Set LPR bits for 19.2K baud, 8-level, 2 stop bits, line 0.
160014/000000 1 <↑>	Set TCR bit 00.
160012/0nnnnn <↑>	
160010/100050 <LF>	Check CSR for TRDY set and Tx line = 0.
160012/0nnnnn <LF>	
160014/000001 <LF>	
160016/000000 377 <↑>	Load octal 377 into TDR.
160014/000001 <↑>	
160012/100377 <↑>	Check RBUF for Data Valid set, for OVRN ERR, FRAM ERR, and PAR ERR clear, for Rx line = 0, and for the data to be 377.
160010/100050 <LF>	Check CSR for TRDY set and RDONE cleared.
160012/000377 <LF>	Check RBUF for Data Valid cleared.
160014/000001 <LF>	
160016/000000 252 <↑>	Load octal 252 into TDR.
160014/000001 <↑>	
160012/100252 <↑>	Read RBUF for Data Valid set, the error bits clear, Rx line = 0, and the data to be 252.
160010/100050 <LF>	Check CSR for TRDY set and RDONE cleared.
160012/000252 <LF>	Read RBUF for Data Valid cleared.
160014/000001 <LF>	

160016/000000 125 <↑>	Load octal 125 into TDR.
160014/000001 <↑>	
160012/100125 <↑>	Check RBUF for Data Valid set, no error bits set, Rx line = 0, and the data being 125.
160010/100050 <LF>	Check CSR for TRDY set and RDONE cleared.
160012/000125 <LF>	Read RBUF for Data Valid cleared.
160014/000001 <LF>	
160016/000000 0<↑>	Load a 0 into TDR.
160014/000001<↑>	
160012/100000<↑>	Read RBUF for Data Valid set, no errors, Rx line = 0, and the data bits being 0s.
160010/100050	Check CSR for TRDY set and RDONE cleared.

6. This test sets the maintenance bit but disables the receivers. It then transmits a character and checks to see that it is not received.

@160010/000000 20 <CR>	Set Master Clear.
@/000000 50	Set MSE and MAINT in CSR.
160012/0nnnnn 7470 <LF>	Load the LPR with RX ENAB cleared.
160014/000000 1<↑>	Set TCR bit 00.
160012/0nnnnn <↑>	
160010/100050 <LF>	Check CSR for TRDY set and RDONE cleared.
160012/0nnnnn <LF>	
160014/000001 <LF>	
160016/000000 377 <↑>	Load 377 into TDR.
160014/000001 <↑>	
160012/0nnnnn <↑>	Check RBUF to see that Data Valid did not set.
160010/100050	Check CSR to see that RDONE is clear.

7. This test sets line 0 for 5-level code and then attempts to transmit and receive 377. Transmitted bits are masked in the process, and a 37 is received. This proves that the UARTs have switched to 5-level.

@160010/000000 20 <CR>	Set Master Clear.
@/000000 50 <LF>	Set MSE and MAINT in CSR.
160012/0nnnnn 17400 <LF>	Load LPR for 19.2K baud, 5-level, line number 0.
160014/000000 1 <↑>	Set TCR bit 00.
160012/0nnnnn <↑>	
160010/100050 <LF>	Check CSR for TRDY set and line numbers 0.
160012/0nnnnn <LF>	
160014/000001 <LF>	
160016/000000 377 <↑>	Load 377 into TDR.
160014/000001 <↑>	
160012/100037 <↑>	Read RBUF for Data Valid set, no errors, line = 0, data 37.
160010/100050	Check CSR for TRDY set and RDONE cleared.

APPENDIX A
IC DESCRIPTIONS

A.1 GENERAL

This appendix contains data on the LSI chips used by the DZV11. The other smaller ICs are common, widely-used logic devices. Detailed specifications on these chips are readily available, and hence are not included here.

A.2 UART

The UART is a MOS/LSI device packaged in a 40-pin DIP. It is a complete subsystem that transmits and receives asynchronous data in duplex or half-duplex operation. The receiver and transmitter can operate simultaneously. The transmitter accepts parallel binary characters and converts them to a serial asynchronous output.

The receiver accepts serial asynchronous binary characters and converts them to a parallel output. The receiver and transmitter clocks are separate and must be 16 times the desired baud rate. The allowable clock rate is dc to 160 kHz.

Control bits are provided to select: character lengths of 5, 6, 7, or 8 bits (excluding parity); odd, even, or no parity; and 1 or 2 stop bits for 6-, 7-, or 8-bit characters. For 5-bit characters, 1 or 1-1/2 start bits are used. The format of a typical input/output serial word is shown in Figure A-1.

Both the receiver and transmitter have double character buffering so that at least one complete character is always available. A register is also provided to store control information.

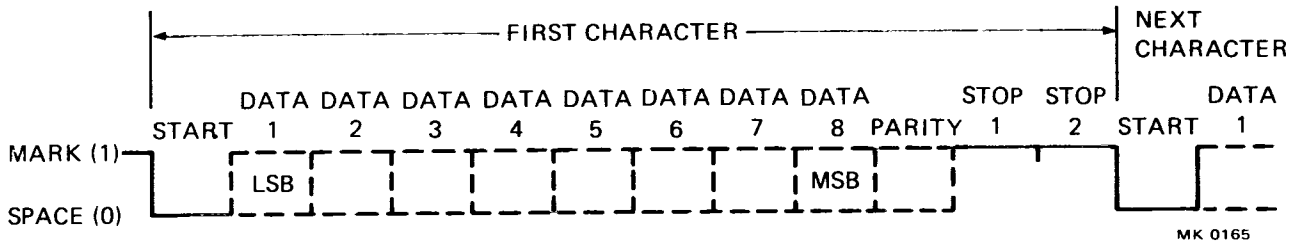
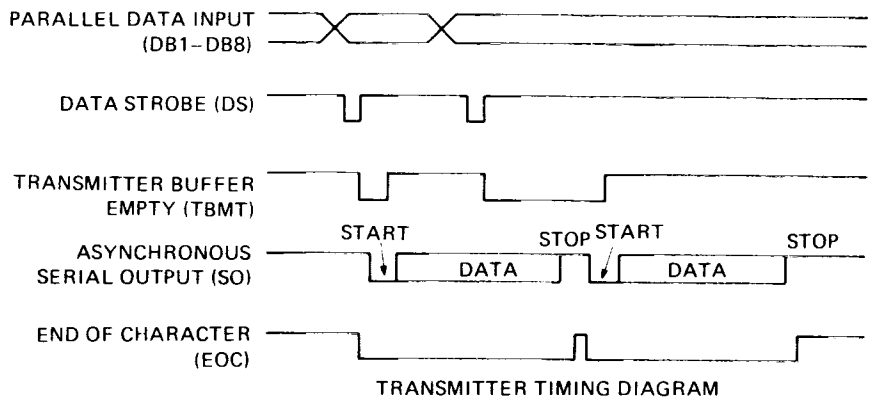


Figure A-1 Format of Typical Serial Character

A block diagram and simplified timing diagram for the UART transmitter are shown in Figure A-2. The transmitter data buffer (holding) register can be loaded with a character when the TBMT (Transmitter Buffer Empty) line goes high. Loading is accomplished by generating a short negative pulse on the DS (Data Strobe) line. The positive-going trailing edge of the DS pulse performs the load operation. The character is automatically transferred to the UART transmitter shift register when this



TRANSMITTER TIMING DIAGRAM

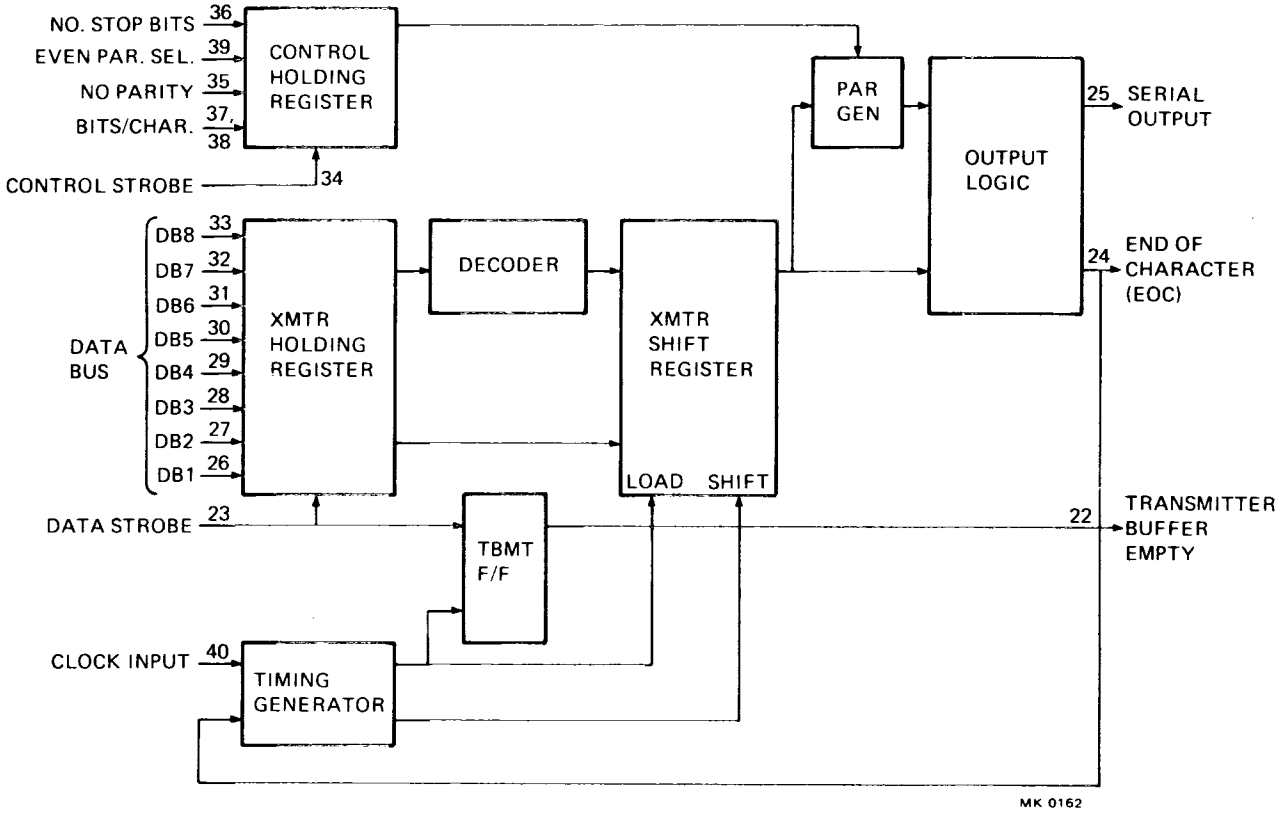


Figure A-2 UART Transmitter

register becomes empty. The desired start, stop and parity bits are added to the data and transmission begins. One-sixteenth of a bit time before a complete character (included stop bits) has been transmitted, the EOC (End-of-Character) line goes high and remains in this state until transmission of a new character begins.

A block diagram and simplified timing diagram for the UART receiver are shown in Figure A-3. Serial asynchronous data is sent to the SI (Serial Input) line. The UART searches for a high-to-low (mark-to-space) transition on the SI line. If this transition is detected, the receiver looks for the center of the start bit as the first sampling point. If this point is low (space), the signal is assumed to be a valid start bit and sampling continues at the center of the subsequent data and stop bits. The character is assembled bit by bit in the receiver shift register in accordance with the control signals that determine the number of data bits and stop bits and the type of parity, if selected. If parity is selected and does not check, the RPE (Receiver Parity Error) line goes high. If the first stop bit is low, the FER (Framing Error) line goes high. After the stop bit is sampled, the receiver transfers in parallel the contents of the receiver shift register into the receiver data buffer (holding) register. The receiver then sets the DA (Received Data Available) line and transfers the state of the framing error bits to the status holding register. When the module accepts the receiver output, it drives the RDA (Reset Data Available) line low which clears the DA line. If this line is not reset before a new character is transferred to the receiver holding register, the OR (Overrun) line goes high and is held there until the next character is loaded into the receiver holding register.

Figure A-4 is a pin/signal designation diagram for the UART. The function of each signal is given in Table A-1. In the function column, the references to high and low signals are with respect to the pins on the UART.

Table A-1 UART Signal Functions

Pin Number	Mnemonic	Name	Function
1	V_{cc}	+5 V	Power Supply
2	V_{gg}	-12 V	Power Supply (Later designs do not use this pin.)
3	G	Ground	Ground
4	RDE	Received Data Enable	A logic low on this line places the received data onto the output lines.
5–12	RD1–RD8	Received Data	Eight data out lines that can be wire ORed. RD8 (pin 5) is the MSB and RD1 (pin 12) is the LSB. When 5, 6, or 7, bits are low. Character is right justified into the least significant bits.
13	PER	Receiver Parity Error	Goes high if the received character parity does not agree with the selected parity.
14	FER	Framing Error	Goes high if the received character has no valid stop bit.

Table A-1 UART Signal Functions (Cont)

Pin Number	Mnemonic	Name	Function
15	OR	Overrun	Goes high if the previously received character is not read (DA line not reset) before the present character is transferred to the receiver holding register.
16	SWE	Status Word Enable	When low, places the status word bits (PE, OR, TMBT, FE, and DA) on the output lines.
17	RCP	Receiver Clock	Input for an external clock whose frequency must be 16 times the desired receiver baud rate.
18	RDA	Reset Data	When low, resets the received DA (data available) line.
19	DA	Received Data	Goes high when an entire character has been received and transferred to the receiver holding register.
20	SI	Serial Input	Input for serial asynchronous data.
21	XR	External Reset	After power is turned on, this line should be pulsed high which resets all registers, sets serial output line high, sets end-of-character line high, and sets transmitter buffer empty line high.
22	TBMT	Transmitter Buffer Empty	Goes high when the transmitter data holding register may be loaded with another character.
23	DS	Data Strobe	Pulsed low to load the data bits into the transmitter data holding register during the positive-going trailing edge of the pulse.
24	EOC	End-of-Character	Goes high each time a full character, including stop bits, is transmitted. It remains high until transmission of the next character starts. This is defined as the mark (high) to space (low) transition of the start bit. This line remains high when no data is being transmitted. When full speed transmission occurs, this lead goes high for 1/16 bit time at the end of each character.

Table A-1 UART Signal Functions (Cont)

Pin Number	Mnemonic	Name	Function
25	SO	Serial Output	Output for transmitted character in serial asynchronous format. A mark is high and a space is low. Remains high when no data is being transmitted.
26–33	DB1–DB8	Data Input	Eight parallel data-in lines. DB8 (pin 33) is the MSB and DB1 (pin 26) is the LSB. If 5-, 6-, or 7-bit characters are selected, the least significant bits are used.
34	CS	Control Strobe	When high, places the control bits (POE, NP, SB, NB1, and NB2) into the control bits holding register.
35	NP	No Parity	When high, eliminates the parity bit from the transmitted and received character and drives the received Parity Error (PER) line low. As a result, the receiver does not check parity on reception and during transmission. The stop bits immediately follow the last data bit.
36	2 SB	Two Stop Bits	Selects the number of stop bits that immediately follow the parity bit. A low inserts 1 stop bit. A high inserts 1.5 stop bits for 5-character formats and 2 stop bits for other character lengths.
37, 38	NB2, NB1	Number of bits per character (excluding parity)	Select 5, 6, 7, or 8 data bits per character as follows. **Bits/Char** / **NB2 (37)** / **NB1 (38)** 5 / L / L 6 / L / H 7 / H / L 8 / H / H
39	POE	Even Parity Select	Selects the type of parity to be added during transmission and checked during reception. A low selects odd parity and a high selects even parity.
40	TCP	Transmitter Clock	Input for an external clock whose frequencey must be 16 times the desired transmitter baud rate.

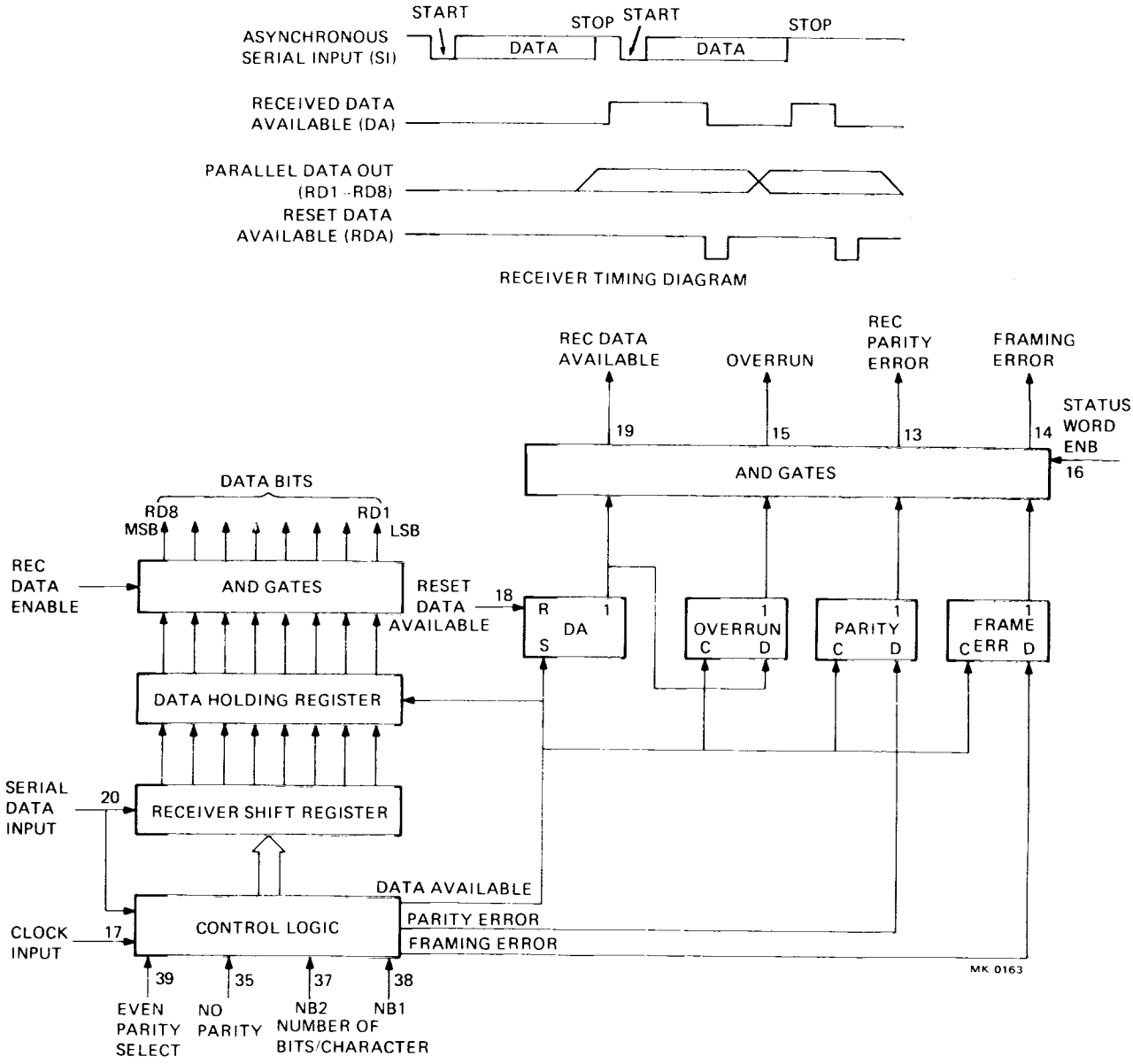


Figure A-3 UART Receiver

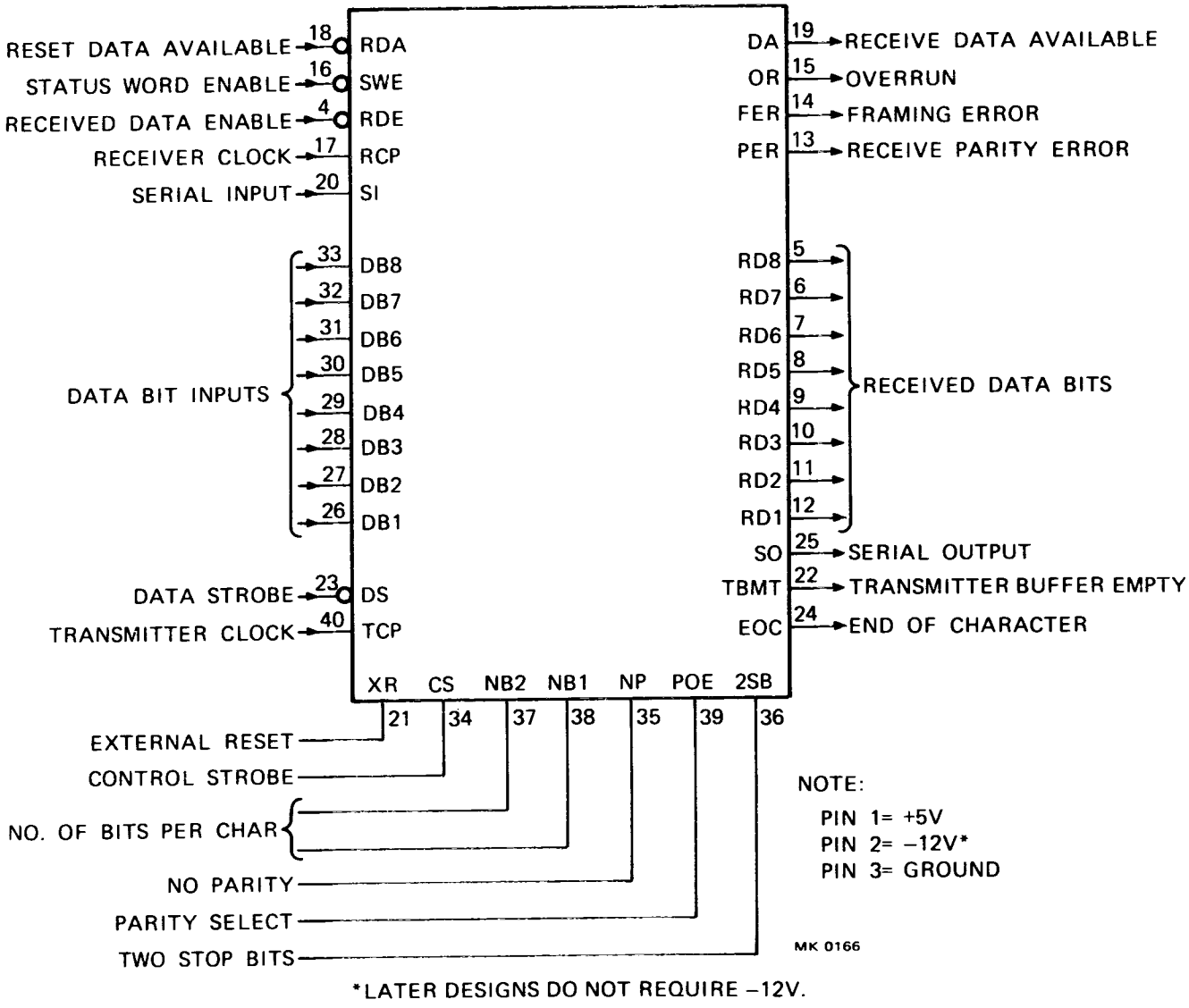


Figure A-4 UART Chip Pin Designations

A.3 DC003 INTERRUPT CHIP

The interrupt chip is an 18-pin DIP device that provides the circuits to perform an interrupt transaction in a computer system that uses a "pass-the-pulse" type arbitration scheme. The device provides two interrupt channels labeled A and B, with the A section at a higher priority than the B section. Bus signals use high-impedance input circuits or high-drive open-collector outputs, which allow the device to directly attach to the computer system bus. Maximum current required from the V_{cc} supply is 140 mA.

Figure A-5 is a simplified logic diagram of the DC003 IC. Timing for the interrupt section is shown in Figure A-6, while Figure A-7 shows the timing for both A and B interrupt sections. Table A-2 describes the signals and pins of the DC003 by pin and signal name.

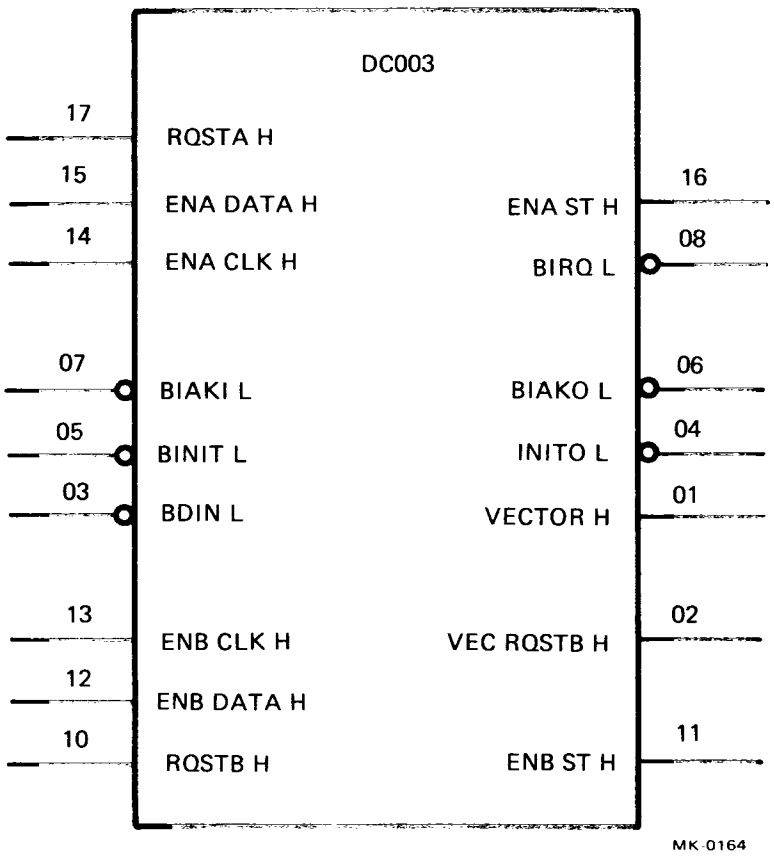


Figure A-5 DC003 Logic Symbol

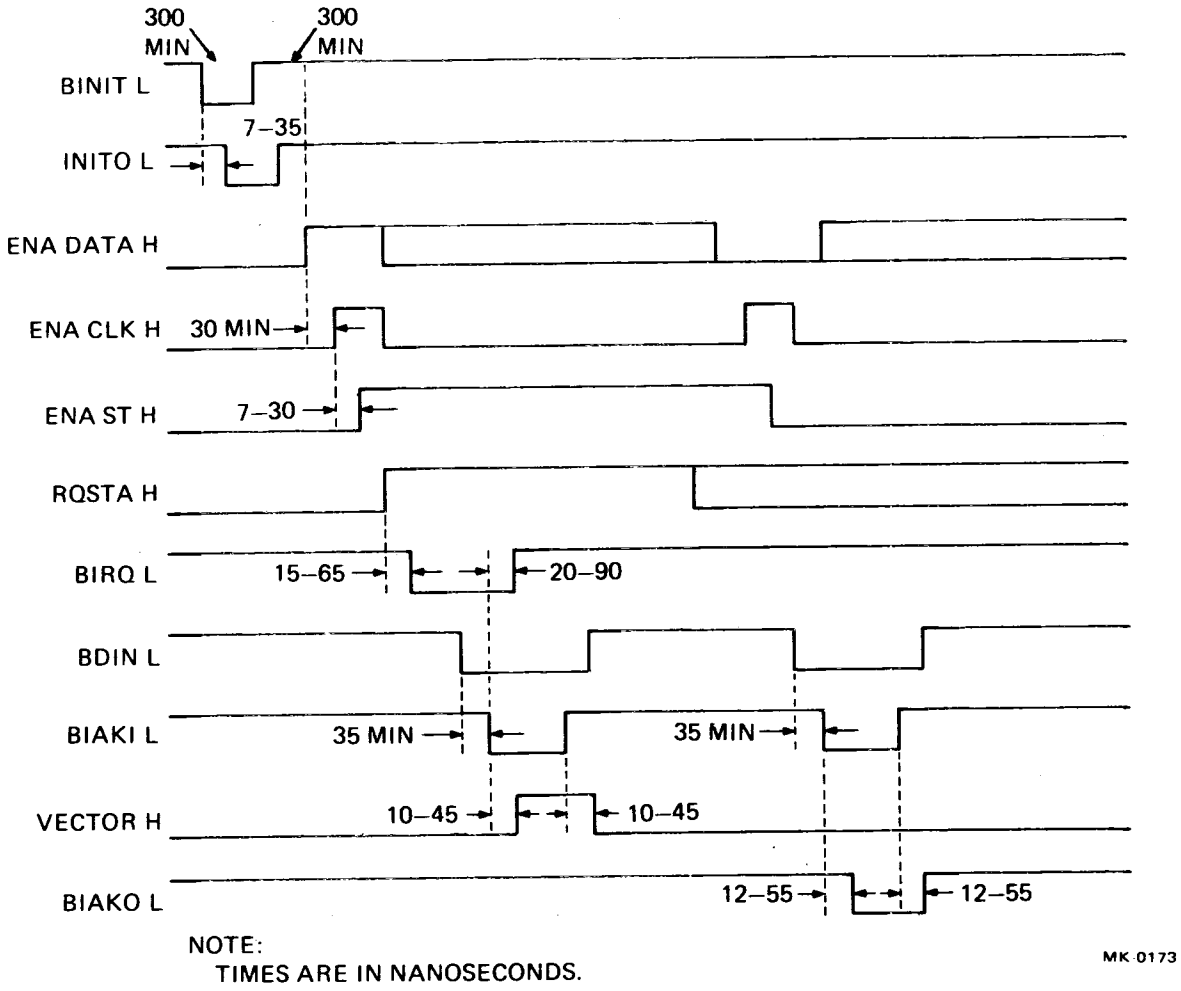
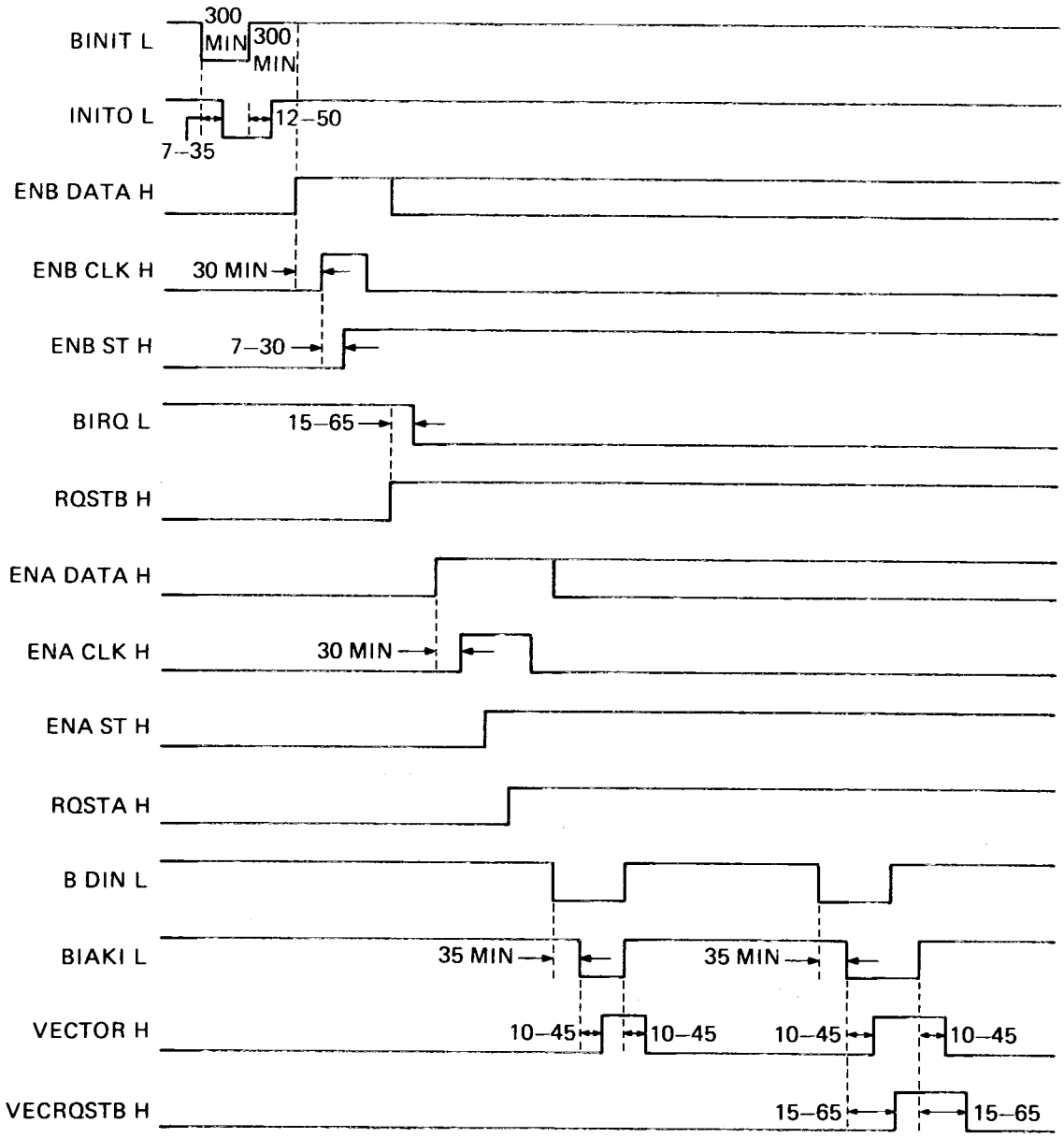


Figure A-6 DC003 A Section Timing



NOTE:
TIMES ARE IN NANOSECONDS.

Figure A-7 DC003 A and B Section Timing

Table A-2 DC003 Signals

Pin Number	I/O Name	Symbol	Function
1	Interrupt Vector Gating Signal	VECTOR H	This signal gates the appropriate vector address onto the bus and to form the bus signal BRPLY L.
2	Vector Request B Signal	VEC RQSTB H	When asserted, this signal indicates RQST B service vector address is required. When negated, it indicates RQST A service vector address is required. VECTOR H is the gating signal for the entire vector address; VEC RQST B H is normally bit 2 of the address.
3	Bus Data In	BDIN L	THE BDIN signal always precedes a BIAK signal.
4	Initialize Out	INITO L	This is the buffered BINIT L signal used in the device interface for general initialization.
5	Bus Initialize	BINIT L	When asserted, this signal brings all drive lines to their negated state (except INITO L).
6	Bus Interrupt Acknowledge	BIAKO L	This signal is the daisy-chained signal that is passed by all devices not requesting interrupt service (see BIAKI L). Once passed by a device, it must remain passed until a new BAIKI L is generated.
7	Bus Interrupt Acknowledge	BIAKI L	This signal is the processor's response to BIRQ L true. This signal is daisy-chained such that the first requesting device blocks the signal propagation while non-requesting devices pass the signal on as BIAKO L to the next device in the chain. The leading edge of BIAKI L causes BIRQ L to be unasserted by the requesting device.
8	Asynchronous Bus Interrupt Request	BIRQ L	The request is generated by a true RQST signal along with the associated true Interrupt Enable signal. The request is removed after the acceptance of the BDIN L signal and on the leading edge of the BAIKI L signal, or the removal of the associated interrupt enable, or due to the removal of the associated request signal.

Table A-2 DC003 Signals (Cont)

Pin Number	I/O Name	Symbol	Function
17 10	Device Interrupt Request Signal	RQSTA H RQSTB H	When asserted with the enable A/B flip-flop asserted, this signal causes the assertion of BIRQ L on the bus. This signal line normally remains asserted until the request is serviced.
16 11	Interrupt Enable Status	ENA ST H ENB ST H	This signal indicates the state of the interrupt enable A/B internal flip-flop which is controlled by the signal line ENA/B DATA H and the ENA/B CLK H clock line.
15 12	Interrupt Enable Data	ENA DATA H ENB DATA	The level on this line, in conjunction with the ENA/B CLK H signal, determines the state of the internal interrupt enable A flip-flop. The output of this flip-flop is monitored by the ENA/B ST H signal.
14 13	Interrupt Enable Clock	ENA CLK H ENB CLK H	When asserted (on the positive edge), interrupt enable A/B flip-flop assumes the state of the ENA/B DATA H signal line.

A.4 DC004 PROTOCOL CHIP

The protocol chip is a 20-pin DIP device that functions as a register selector, providing the signals necessary to control data flow into and out of up to four word registers (8 bytes). Bus signals can directly attach to the device because receivers and drivers are provided on the chip. An RC delay circuit is provided to slow the response of the peripheral interface to data transfer requests. The circuit is designed such that if tight tolerance is not required, then only an external 1K ±20 percent resistor is necessary. External RCs can be added to vary the delay. Maximum current required from the V_{cc} supply is 120 mA.

Figure A-8 is a simplified logic diagram of the DC004 IC. Signal timing with respect to different loads are tabularized in Table A-3 and are shown in Figure A-9. Figure A-10 shows the loading for the test conditions in Table A-3. Signal and pin definitions for the DC004 are presented in Table A-4.

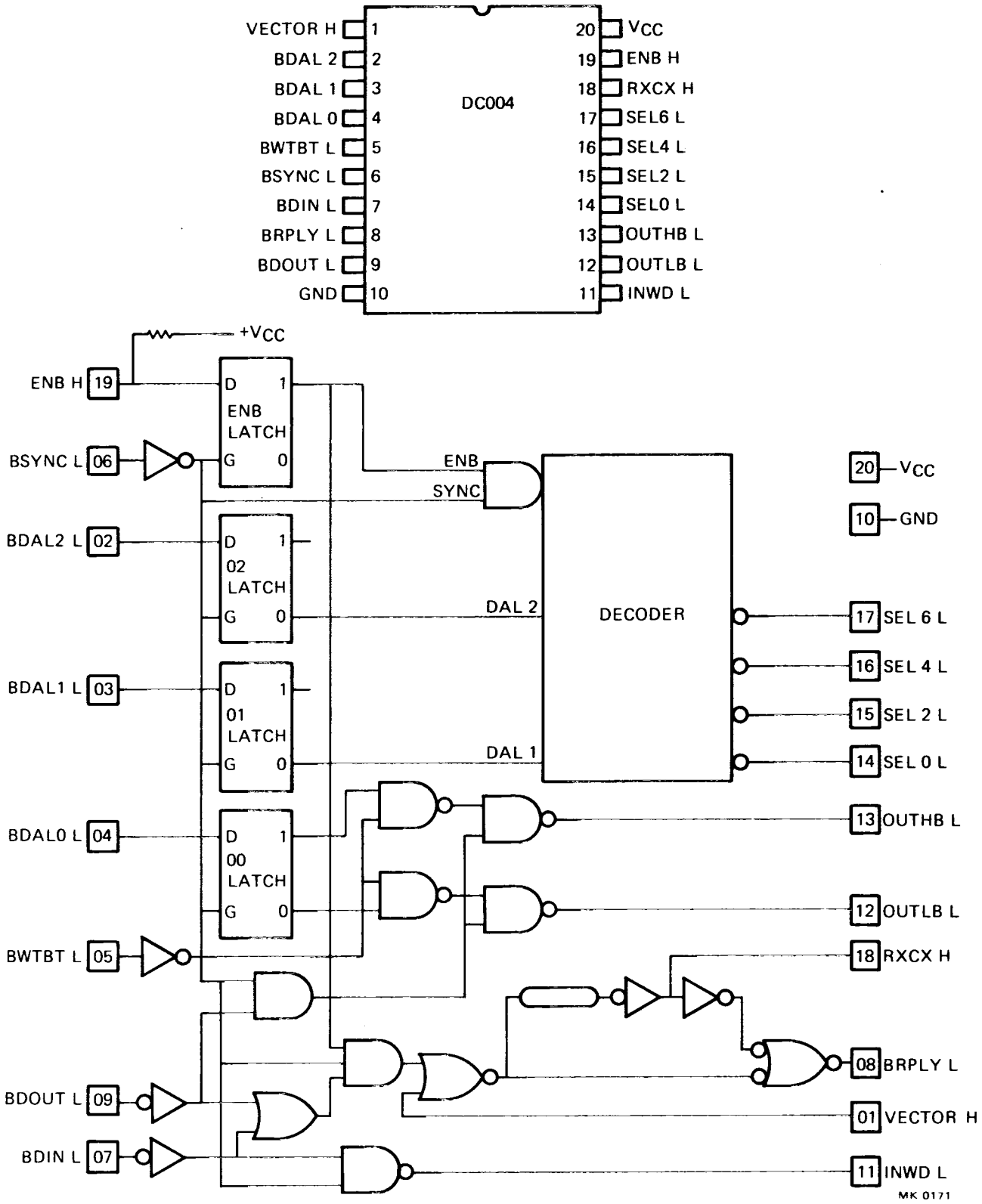
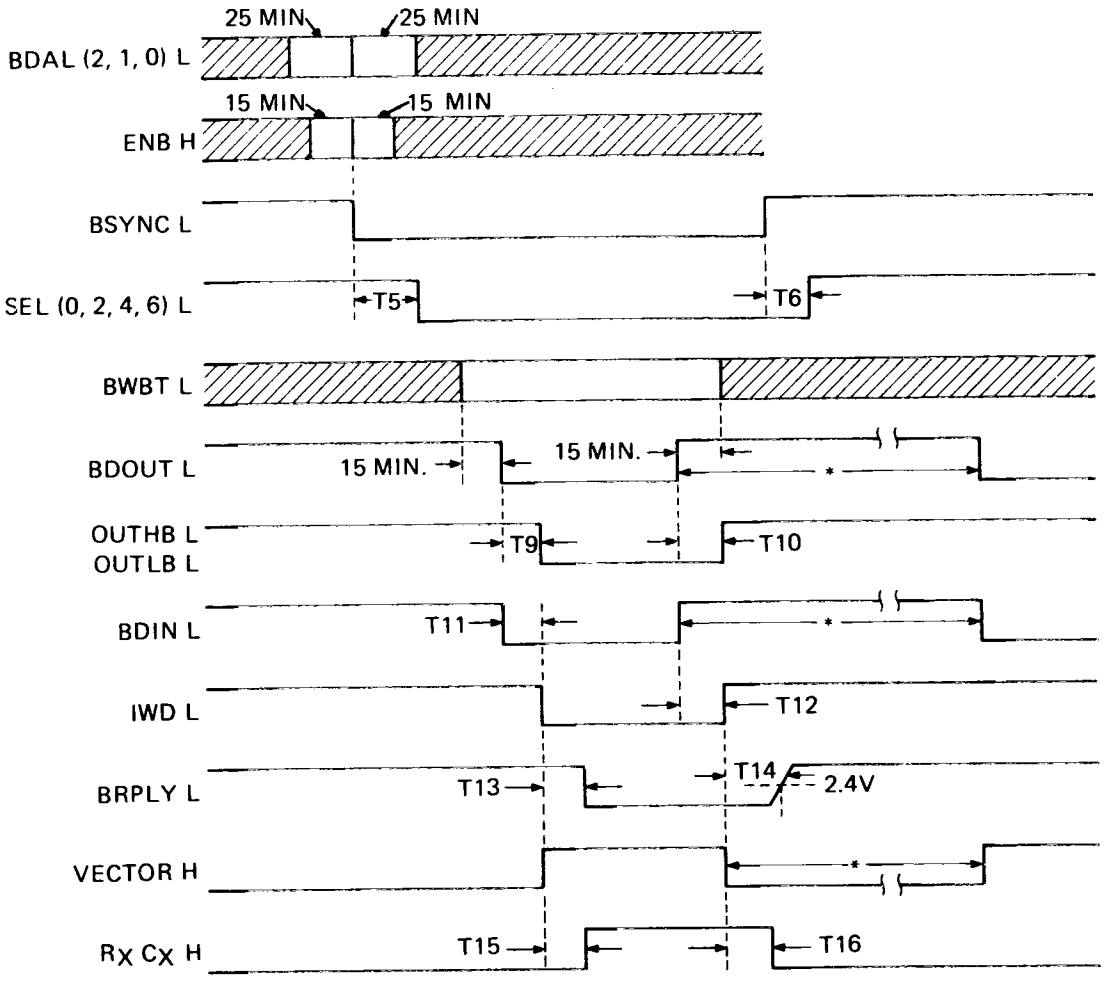


Figure A-8 DC004 Simplified Logic Diagram

Table A-3 DC004 Signal Timing versus Output Loading

	With Respect To		Test Condition	Output Being Asserted		Output Being Negated		Figure A-10 Reference
	Signal	Signal		Min (ns)	Max (ns)	Min (ns)	Max (ns)	
	SEL n L (n = 0, 2, 4, 6)	B$YNC L	Load B Load C	15 15	35 40	5 5	25 30	t_5, t_6
	OUTLB L	BDOUT L	Load B Load C	5 5	25 30	5 5	25 30	t_9, t_{10}
	OUTHB L	DBOUT L	Load B Load C	5 5	25 30	5 5	25 30	t_9, t_{11}
	INWD L	BDIN L	Load A Load B	5 5	25 30	5 5	25 30	t_{11}, t_{12}
Pin 18 Connection RX = 1K ±5% 350 ±5% 15 pF ±5%	BRPLY L (Load A)	OUTLB L (Load B)		20	60	-10	45	t_{13}, t_{14}
	BRPLY L (Load A)	OUTHB L (Load B)		20	60	-10	45	t_{13}, t_{14}
	BRPLY L (Load A)	INWD L (Load B)		20	60	-10	45	t_{13}, t_{14}
	BRPLY L	VECTOR H (Load A)		30	70	0	45	t_{13}, t_{14}
Pin 18 Connection RX = 4.64K ±1%	BRPLY L (Load A)	OUTLB L (Load B)		300	400	-10	45	t_{13}, t_{14}
	BRPLY L (Load A)	OUTHBL (Load B)		300	400	-10	45	t_{13}, t_{14}
CX = 220 pF ±1%	BRPLY L (Load A)	INWD L (Load B)		300	400	-10	45	t_{13},t_{14}
	BRPLY L (Load A)	VECTOR H		330	430	0	45	t_{13}, t_{14}



*TIME REQUIRED TO DISCHARGE R_X C_X FROM ANY CONDITION ASSERTED = 150ns

MK 0172

NOTE:
TIMES ARE IN NANOSECONDS.

Figure A-9 DC004 Timing Diagram

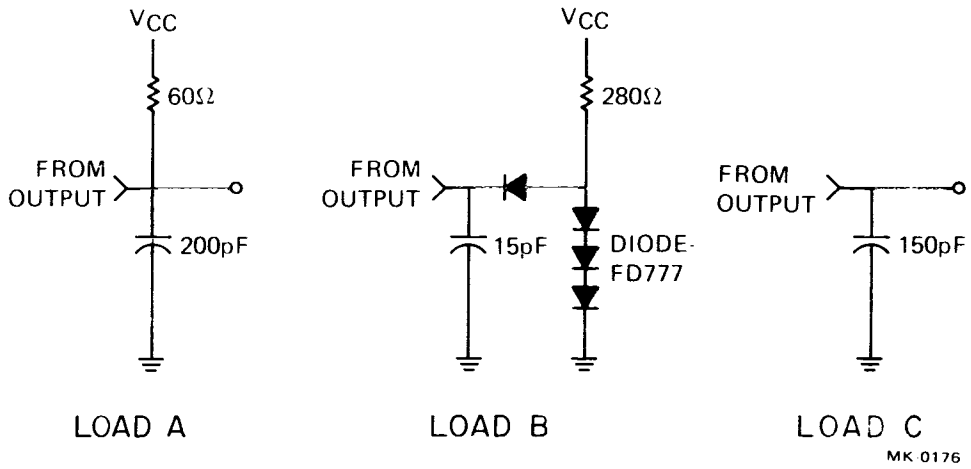


Figure A-10 DC004 Loading Configuration

Table A-4 DC004 Pin/Signal Descriptions

Pin	Signal	Description
1	VECTOR H	Vector – This input causes BRPLY L to be generated through the delay circuit. Independent of BSYNC L and ENB H.
2 3 4	BDAL2 L BDAL1 L BDAL0 L	Bus Data Address Lines – These signals are latched at the assert edge of BSYNC L. Lines 2 and 1 are decoded for the select outputs; line 0 is used for byte selection.
5	BWTBT L	Bus Write/Byte – While the BDOUT L input is asserted, this signal indicates a byte or word operation: asserted = byte, unasserted = word. Decoded with BDOUT L and latched BDAL0 L to form OUTLB L and OUTHB L.
6	BSYNC L	Bus Synchronize – At the assert edge of this signal, address information is trapped in four latches. While unasserted, disables all outputs except the vector term of BRPLY L.
7	BDIN L	Bus Data In – This is a strobing signal to effect a data input transaction. Generates BRPLY L through the delay circuit and INWD L.
8	BRPLY L	Bus Reply – This signal is generated through an RC delay by VECTOR H, and strobed by BDIN L or DBOUT L, and BSYNC L and latched ENB H.

Table A-4 DC004 Pin/Signal Descriptions (Cont)

Pin	Signal	Description
9	BDOUT L	Bus Data Out – This is a strobing signal to effect a data output transaction. Decoded with BWTBT L and BDALO to form OUTLB L and OUTHB L. Generates BRPLY L through the delay circuit.
11	INWDL	In Word – Used to gate (read) data from a selected register onto the data bus. Enabled by BSYNC L and strobed by BDIN L.
12 13	OUTHB L OUTLB L	Out Low Byte, Out High Byte – Used to load (write) data into the lower, higher, or both bytes of a selected register. Enabled by BSYNC L and decode of BWTBT L and latched BDAL0 L, and strobed by BDOUT L.
14 15 16 17	SEL0 L SEL2 L SEL4 L SEL6 L	Select Lines – One of these four signals is true as a function of BDAL2 L and BDAL1 L if ENB H is asserted at the assert edge of BSYNC L. They indicate that a word register has been selected for a data transaction. These signals never become asserted except at the assertion of BSYN L (then only if ENB H is asserted at that time) and, once asserted, are not negated until BSYNC L is negated.
18	RXCX	External Resistor Capacitor Node – This node is provided to vary the delay between the BDIN L, BDOUT L, and VECTOR H inputs and BRPLY L output. The external resistor should be tied to V_{cc} and the capacitor to ground. As an output, it is the logical inversion of BRPLY L.
19	ENB H	Enable – This signal is latched at the asserted edge of BSYNC L and is used to enable the select outputs and the address term of BRPLY L.

A.5 DC005 BUS TRANSCEIVER CHIP

The 4-bit transceiver is a 20-pin DIP, low-power Schottky device for primary use in peripheral device interfaces, functioning as a bidirectional buffer between a data bus and peripheral device logic. In addition to the isolation function, the device also provides a comparison circuit for address selection and a constant generator, useful for interrupt vector addresses. The bus I/O port provides high-impedance inputs and high-drive (70 mA) open-collector outputs to allow direct connection to a computer's data bus. On the peripheral device side, a bidirectional port is also provided, with standard TTL inputs and 20 mA tri-state drivers. Data on this port is the logical inversion of the data on the bus side.

Three address jumper inputs are used to compare against three bus inputs and to generate the signal MATCH. The MATCH output is open-collector, which allows the output of several transceivers to be wire-ANDed to form a composite address match signal. The address jumpers can also be put into a third logical state that disconnects that jumper from the address match, allowing for "don't care" address bits. In addition to the three address jumper inputs, a fourth high-impedance input line is used to enable/disable the MATCH output.

Three vector jumper inputs are used to generate a constant that can be passed to the computer bus. The three inputs directly drive three of the bus lines, overriding the action of the control lines.

Two control signals are decoded to give three operational states: receiver data, transmit data, and disable.

Maximum current required from the V_{cc} supply is 100 mA.

Figure A-11 is a simplified logic diagram of the DC005 IC. Timing for the various functions is shown in Figure A-12. Signal and pin definitions for the DC005 are presented in Table A-5.

Table A-5 DC005 Pin/Signal Descriptions

Pin	Name	Function
12 11 9 8	BUS 0 L BUS 1 L BUS 2 L BUS 3 L	Bus Data – This set of four lines constitutes the bus side of the transceiver. Open-collector outputs; high-impedance inputs. Low = 1.
18 17 7 6	DAT 0 H DAT 1 H DAT 2 H DAT 3 H	Peripheral Device Data – These four tri-state lines carry the inverted received data from BUS (3:0) when the transceiver is in the receive mode. When in transmit data mode, the data carried on these lines is passed inverted to BUS (3:0). When in the disabled mode, these lines go open (hi-Z). High = 1.
14 15 16	JV 1 H JV 2 H JV 3 H	Vector Jumpers – These inputs, with internal pull-down resistors, directly drive BUS (3:1). A low or open on the jumper pin causes an open condtion on the corresponding BUS pin if XMIT H is low. A high causes a one (low) to be transmitted on the BUS pin. Note that BUS 0 L is not controlled by any jumper input.
13	MENB L	Match Enable – A low on this line enables the MATCH output. A high forces MATCH low, overriding the match circuit.
3	MATCH H	Address Match – When BUS (3:1) matches with the state of JA (3:1) and MENB L is low, this output is open; otherwise, it is low.

Table A-5 DC005 Pin/Signal Descriptions (Cont)

Pin	Name	Function
1 2 19	JA 1 L JA 2 L JA 3 L	Address Jumpers – A strap to ground on these inputs allows a match to occur with a one (low) on the corresponding BUS line; an open allows a match with a zero (high); a strap to V_{cc} disconnects the corresponding address bit from the comparison.
5	XMIT H	Control Inputs – These lines control the operational of the transceiver as follows.
4	REC H	REC XMIT 0 0 DISABLE: BUS and DAT open 0 1 XMIT DATA: DAT to BUS 1 0 RECEIVE: BUS to DAT 1 1 RECEIVE: BUS to DAT To avoid tri-state overlap conditions, an internal circuit delays the change of modes between XMIT DATA mode, and delays tri-state drivers on the DAT lines from enabling. This action is independent of the DISABLE mode.

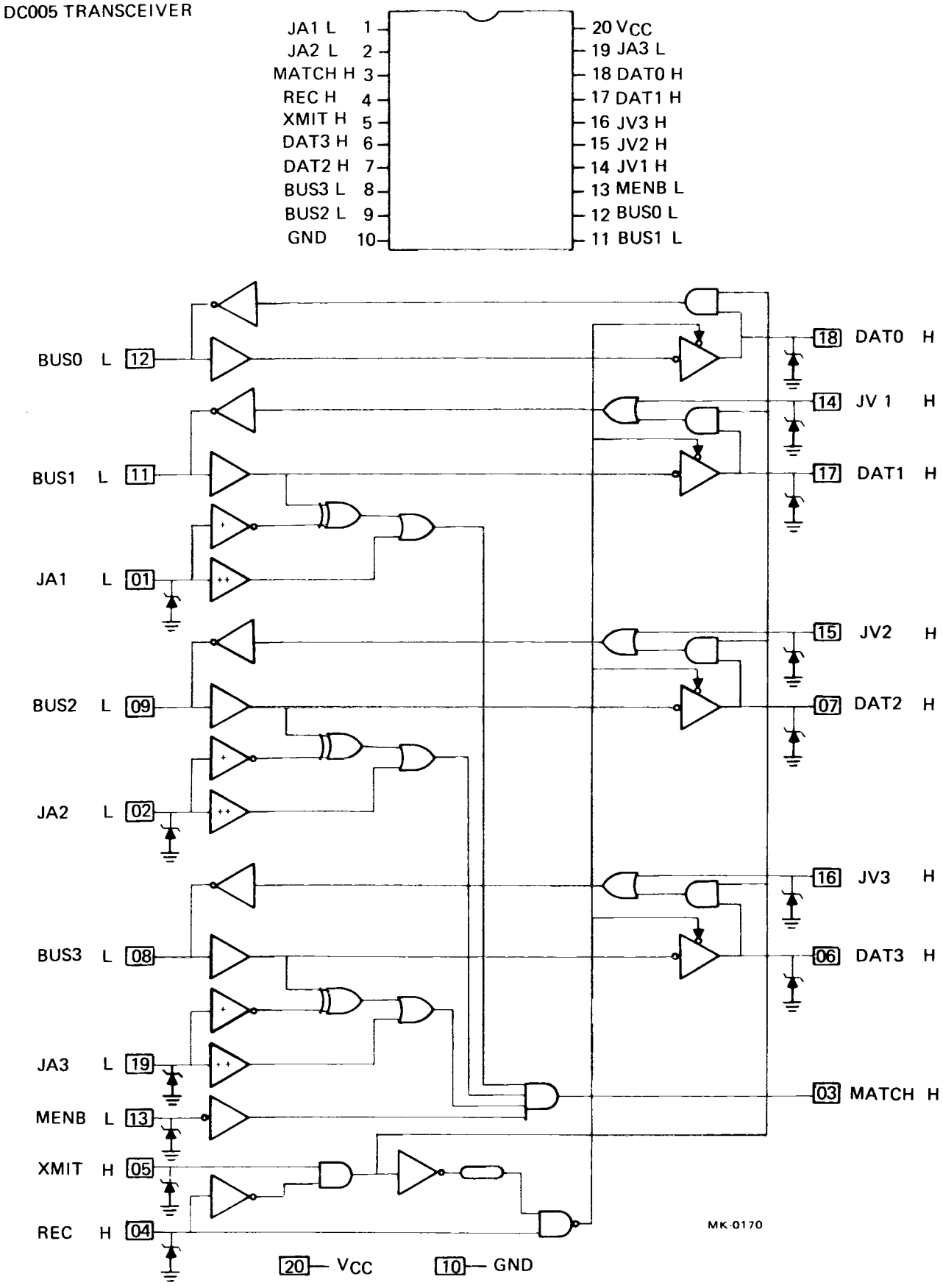


Figure A-11 DC005 Simplified Logic Diagram

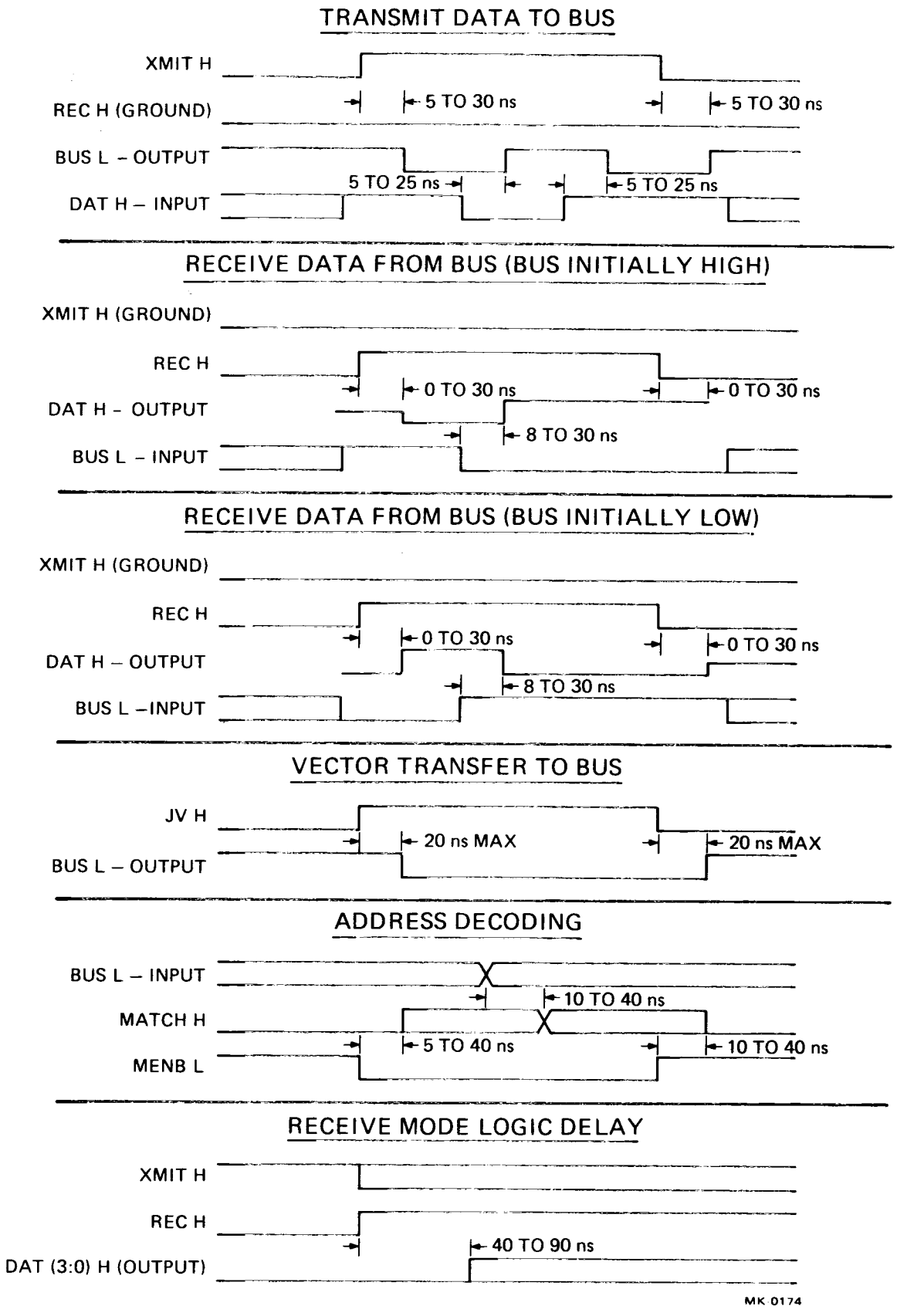


Figure A-12 DC005 Timing Diagram

A.6 COM 5016 DUAL BAUD RATE GENERATOR

The 5016 is an LSI MOS device containing two independent sections. Each section divides its input clock frequency by one of 16 divisors to produce one of 16 different clock outputs. The divisors are stored in ROMs on the chip. The ROMs are addressed by circuits that latch in and decode the logical states of the address lines (Figure A-13). The address lines may be strobed or held at a dc level. Table A-6 lists the frequencies selected by the address lines. Figure A-14 depicts the 5016 pin locations. Table A-7 defines their functions.

A.7 3341 FIFO SERIAL MEMORY

The 3341 first-in/first-out memory chip asserts Input Ready when it is ready to load data. Each time Shift In is asserted, the chip accepts 4 bits of parallel data and shifts them to the output end of a 64- × 4-bit register. It then asserts Output Ready. When Shift Out is asserted, the chip places the data in the output latches (Figure A-15).

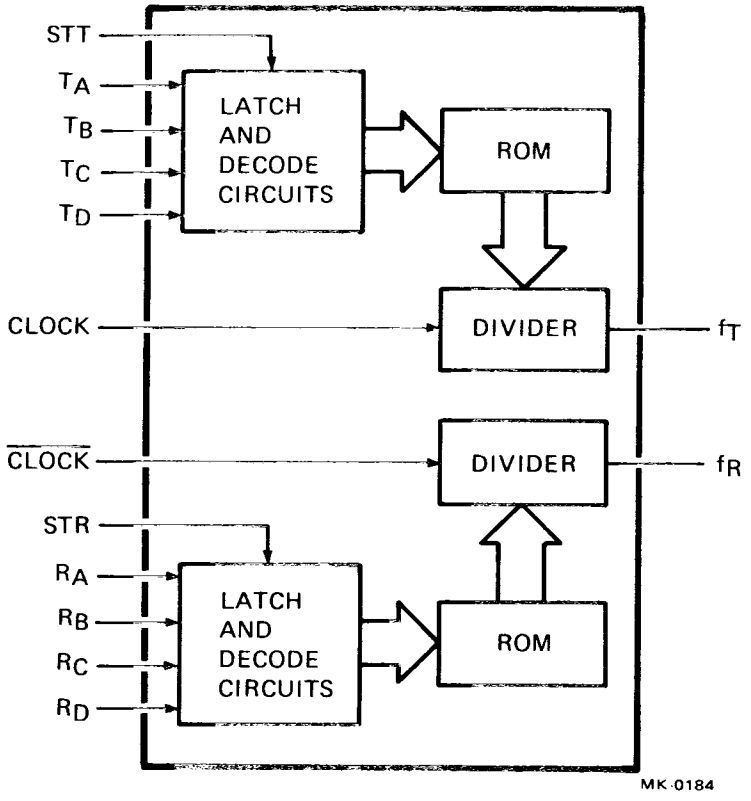


Figure A-13 COM 5016 Simplified Block Diagram

Table A-6 COM 5016 Selectable Frequencies

Transmit/Receive Address				Baud Rate	Frequency 16×Clock (kHz)	Divisor
D	C	B	A			
0	0	0	0	50	0.8	6336
0	0	0	1	75	1.2	4224
0	0	1	0	110	1.76	2880
0	0	1	1	134.5	2.1523	2355
0	1	0	0	150	2.4	2112
0	1	0	1	300	4.8	1056
0	1	1	0	600	9.6	528
0	1	1	1	1200	19.2	264
1	0	0	0	1800	28.8	176
1	0	0	1	2000	32.081	158
1	0	1	0	2400	38.4	132
1	0	1	1	3600	57.6	88
1	1	0	0	4800	76.8	66
1	1	0	1	7200	115.2	44
1	1	1	0	9600	153.6	33
1	1	1	1	19800	316.8	16

Crystal Frequency = 5.0688 MHz

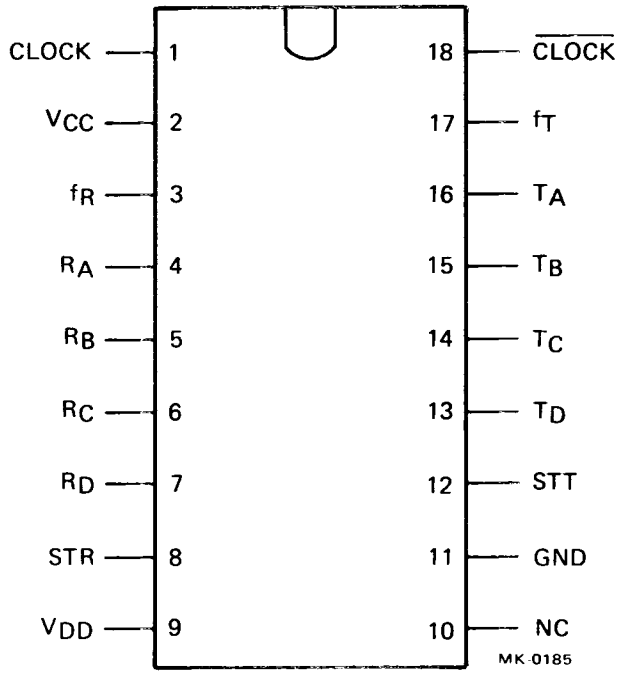


Figure A-14 COM 5016 Pin Locations

Table A-7 COM 5016 Pin Functions

Pin Number	Mnemonic	Name	Function
1	CLOCK (XTAL/EXT1)	External Clock Input	This input is either one pin of a crystal oscillator package or one polarity of another external input.
2	V_{cc}	Power Supply	+5 V supply
3	f_R	Receiver Output Frequency	This output runs at the frequency selected by the receiver address.
4–7	R_A ,R_B	Receiver Address	The logic levels on these inputs select the receiver output frequency, f_R.
8	STR	Strobe-Receiver Address	A high-level input strobe loads the receiver address (R_A, R_B, R_C, R_D) into the latch and decode circuits. This input may be strobed or hard-wired to a high level.
9	V_{DD}	Power Supply	+12 V supply
10	NC	No Connection	
11	GND	Ground	Ground
12	STT	Strobe-Transmitter Address	A high-level input strobe loads the transmitter address (T_A, T_B, T_C, T_D) into the latch and decode circuits. This input may be strobed or hard-wired to a high level.
13–16	TD, TC, TB, TA	Transmitter Address	The logic levels on these inputs select the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at the frequency selected by the transmitter address.
18	CLOCK (XTAL/EXT2)	Inverted External Clock Input	This input is either one pin of a crystal oscillator package or one polarity of another external input.

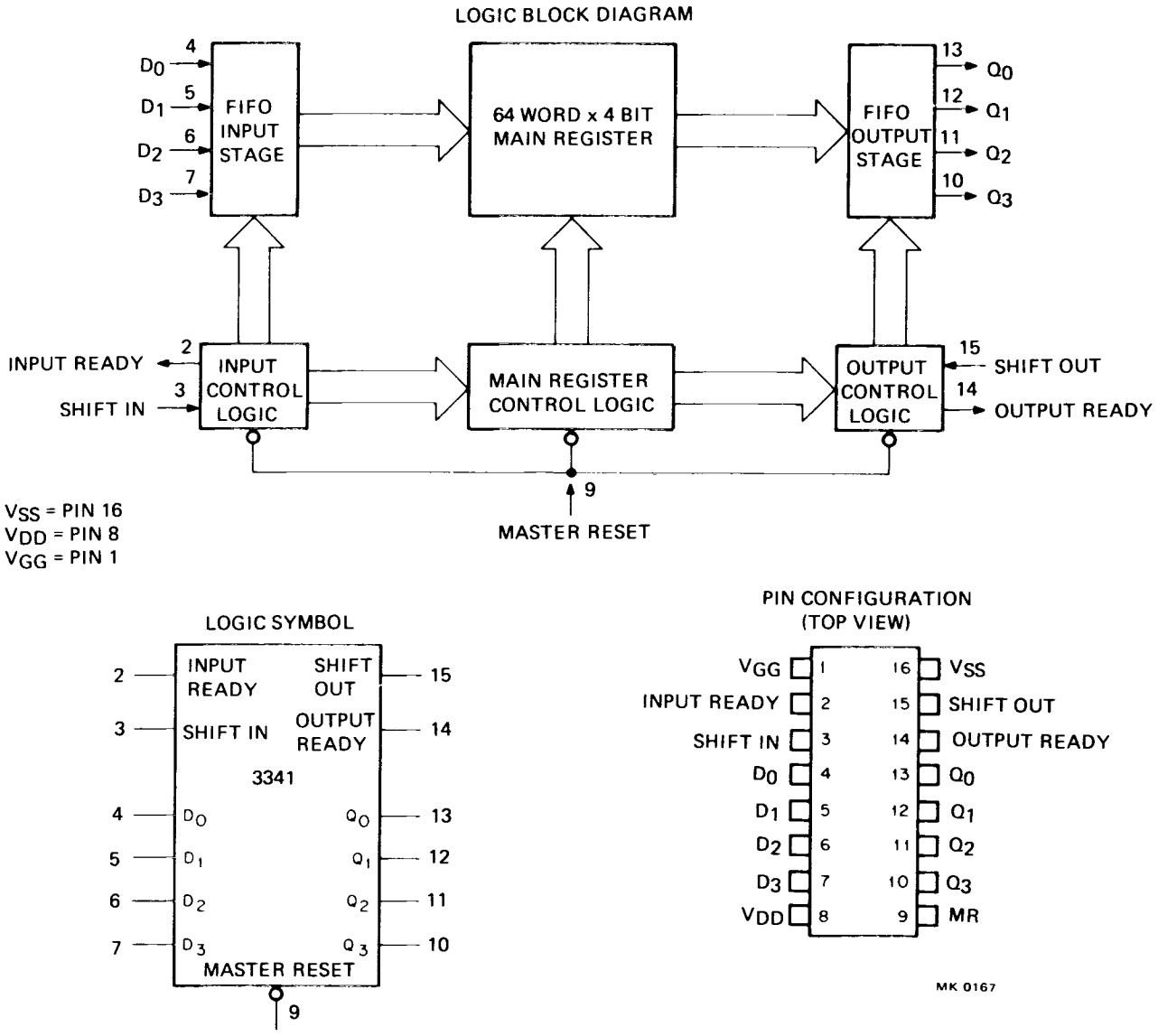


Figure A-15 3341 FIFO Serial Memory

APPENDIX B
CONNECTOR PINNING

Table B-1 lists the DZV11 header connector pinning. Table B-2 lists the edge connector pinning (Figure B-1). Table B-1 also lists the pinning of the BC11U interface cable, and the color of the wires. Note that the wiring sequence does not simply repeat itself for each of the four cable connectors. Instead, the sequence appears twice and then its mirror image is repeated twice. The header connector is wired this way to prevent damage to the EIA transmitters and receivers in the event that the connector is reversed. Reversing the connector, however, reverses the line numbers. Observe the "This Side Up" sticker on the connector.

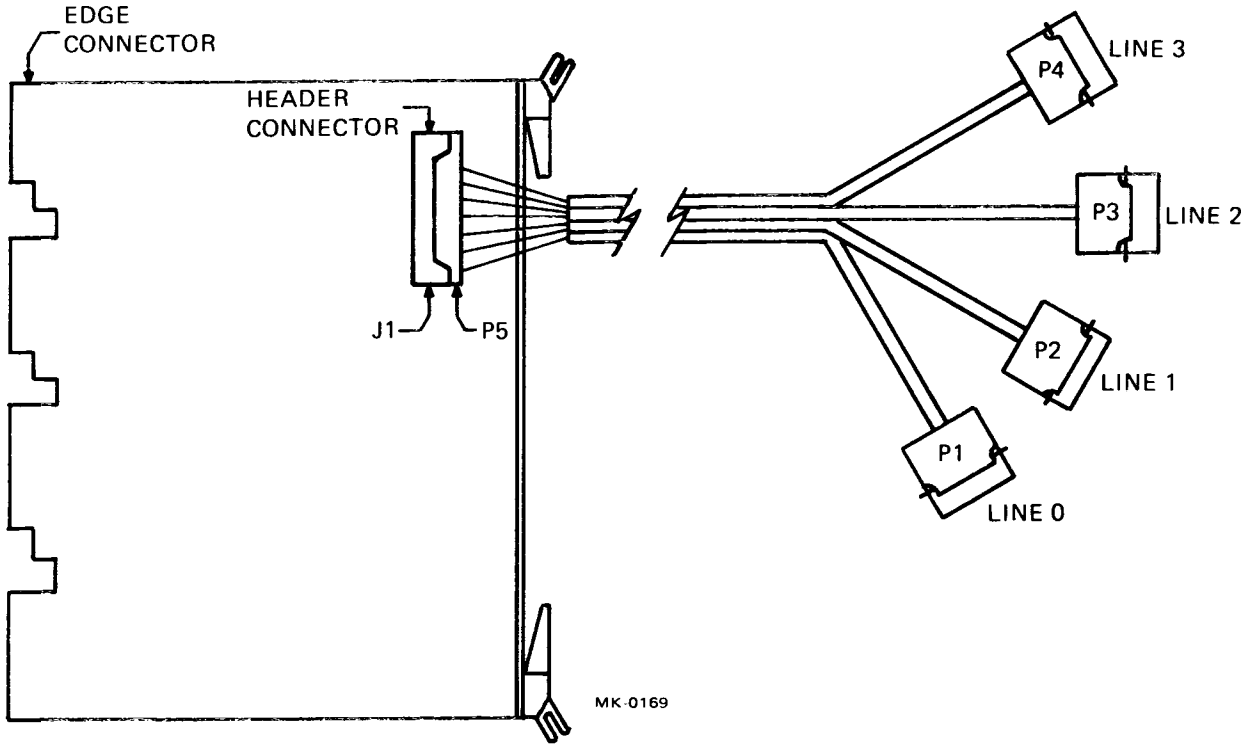


Figure B-1 Connectors

Table B-1 Connector Pinning

EIA Signal Description	Header (Berg) Connector Pin	BC11U Cable Connector Pin		Wire Color
		P5	P1	
Ground	A	A	1	Black
Transmitted Data 00	B	B	2	Brown
Received Data 00	C	C	3	Gray
Data Terminal Ready 00	D	D	20	White
Ring 00	E	E	22	Green
Forced Busy 00	F	F	25	Yellow
Request to Send 00	H	H	4	Blue
	J	J	5	Orange
Ground	K	K	7	Violet
Carrier 00	L	L	8	Red
		P5	**P2**	
Ground	M	M	1	Black
Transmitted Data 01	N	N	2	Brown
Received Data 01	P	P	3	Gray
Data Terminal Ready 01	R	R	20	White
Ring 01	S	S	22	Green
Forced Busy 01	T	T	25	Yellow
Request to Send 01	U	U	4	Blue
	V	V	5	Orange
Ground	W	W	7	Violet
Carrier 01	X	X	8	Red

Table B-1 Connector Pinning (Cont)

EIA Signal Description	Header (Berg) Connector Pin	BC11U Cable Connector Pin		Wire Color
		P5	P3	
Carrier 02	Y	Y	8	Red
Ground	Z	Z	7	Violet
	AA	AA	5	Orange
Request to Send 02	BB	BB	4	Blue
Forced Busy 02	CC	CC	25	Yellow
Ring 02	DD	DD	22	Green
Data Terminal Ready 02	EE	EE	20	White
Received Data 02	FF	FF	3	Gray
Transmitted Data 02	HH	HH	2	Brown
Ground	JJ	JJ	1	Black
		P5	**P4**	
Carrier 03	KK	KK	8	Red
Ground	LL	LL	7	Violet
	MM	MM	5	Orange
Request to Send 03	NN	NN	4	Blue
Forced Busy 03	PP	PP	25	Yellow
Ring 03	RR	RR	22	Green
Data Terminal Ready 03	SS	SS	20	White
Received Data 03	TT	TT	3	Gray
Transmitted Data 03	UU	UU	2	Brown
Ground	VV	VV	1	Black

Table B-2 DZV11 Edge Connector Pinning

Mnemonic	Pin	Mnemonic	Pin
+5	AA2	BDAL14 L	BU2
	BA2	BDAL15 L	BV2
	BV1	BDIN L	AH2
	CA2	BDOUT L	AE2
	DA2	BIAKI L	AM2
+12	BD2	BIAKO L	AN2
BBS7 L	AP2	BINIT L	AT2
BDAL0 L	AU2	BDMGIL	AR2
BDAL1 L	AV2	BDMGOL	AS2
BDAL2 L	BE2	BIRQ L	AL2
BDAL3 L	BF2	BRPLY L	AF2
BDAL4 L	BH2	BSYNC L	AJ2
BDAL5 L	BJ2	BDCOK H	BA1
BDAL6 L	BK2	GND	AC2
BDAL7 L	BL2	GND	AT1
BDAL8 L	BM2	GND	BC2
BDAL9 L	BN2	GND	BT1
BDAL10 L	BP2	W10	CR2
BDAL11 L	BR2		CS2
BDAL12 L	BS2	W11	CM2
BDAL13 L	BT2		CN2

APPENDIX C
GLOSSARY

BBS7 L – Bussed Bank 7 Select (Table 5-1).

BDAL00 L through BDAL15 L - Bussed Data/Address Lines (Table 5-1).

BDIN L – Bussed Data Input (Table 5-1).

BDOUT L – Bussed Data Out (Table 5-1).

BIAKI L – Bussed Interrupt Acknowledge In (Table 5-1).

BIAKO L – Bussed Interrupt Acknowledge Out (Table 5-1).

BINIT L – Bussed Initialize (Table 5-1).

BIRQ L – Bussed Interrupt Request (Table 5-1).

Break – A continuous spacing condition on the serial data line, interpreted as a framing error.

BRK 3 through BRK 0 – TDR bits 11 through 08. When set, the Break bit causes the transmission of a Break signal.

BRPLY L – Bussed Reply (Table 5-1).

BSYNC L – Bussed Sync (Table 5-1).

BWTBT L – Bussed Write Byte (Table 5-1).

Carrier – A carrier is a continuous frequency capable of being modulated or impressed with a signal. The name Carrier, however, is used in the DZV11 print set to refer to the received line signal detector input from the modem. This signal is referred to as "Carrier Detect" and "Carrier On" in some books.

CCITT – The Consultive Committee International Telegraph and Telephone is an advisory committee established under the United Nations to recommend worldwide standards.

CHAR LGTH A, CHAR LGTH B – LPR bits 03 and 04. These bits determine the length of the characters the DZV11 receives and transmits (Table 3-4).

CLR – CSR bit 04. Controls the device Master Clear signal (Table 3-2).

CO – Carrier On. Also referred to as "Carrier" or "Carrier Detect." Some sources abbreviate Carrier Detect to CD. Do not confuse CD or CO with EIA signal CD. EIA signal CD is Data Terminal Ready. The EIA signal designation for Carrier On (or Carrier Detect) is CF.

CO3 through CO0– MSR bits 11 through 08, representing the Carrier signal for lines 03 through 00.

CONTROL STROBE H – This signal is generated by the speed and format control circuits on circuit schematic sheet D8. It loads the speed parameters into the baud rate generators on sheet D8, and loads the data format parameters into the UARTs on sheets D13 and D14.

CSR – Control and Status Register (Table 3-2).

DA00 through DA03 – Data Available. These signals come from the R DONE pins on the UARTs (sheets D13 and D14).

DATA IN 00 H through DATA IN 03 H – These signals are the received data from the EIA signal lines. They originate at the EIA/TTL receivers (sheet D7) and go to the maintenance mode data selector (sheet D10).

DATA TERM RDY 00 through DATA TERM RDY 03 – Data Terminal Ready signals for lines 00 through 03 (sheet D6). Refer to Table 5-2.

Data Valid – Bit 15 in the RBUF. The Output Ready signals from the four silo memory chips are ANDed to form RECEIVER DONE H. When the RBUF is addressed, RECEIVER DONE H is latched as VALID DATA H (sheet D12). VALID DATA H becomes Data Valid (bit 15) in the RBUF.

DATI – Data input bus cycle.

DATIO – Data input/output bus cycle.

DATIOB – Data input/output bus cycle involving a byte.

DATO – Data output bus cycle involving a word.

DATOB – Data output bus cycle involving a byte.

DCE – Data communication equipment.

DEVICE DATA BUS – The bidirectional tri-state bus internal to the module; signal lines DEVICE DATA BUS 00 through DEVICE DATA BUS 15.

DEVICE SELECT H – This signal is the wired-AND of the MATCH signals from all four bus transceiver chips (sheet D2). It enables the protocol chip (sheet D4).

DTE – Data terminal equipment.

DTR – Data Terminal Ready. Refer to Table 5-2.

DTR0 through DTR3 – Bits 08 through 11 in the transmitter control register. They represent the state of Data Terminal Ready for each of the four lines.

EIA – Electronic Industries Association.

FB – Forced Busy. Refer to Table 5-2.

FE00 through FE 03 – Framing Error signals from the UARTs (sheets D13 and D14).

FIFO - First-In/First-Out.

Forced Busy - Used with some modem equipment such as Bell models 103E and 113B. Signals a modem controller to switch to another channel.

FRAM ERR - Framing Error; RBUF bit 13.

Framing Error - This error occurs when a UART receiver does not detect a stop bit at the time it tests for one. This may be caused by a transmission error or by a Break signal.

INITIALIZE H, INITIALIZE L - These are the device initialization signals. They are generated by either the CLR bit (CSR bit 04) or by BINIT from the LSI-11 bus (sheet D5).

LD BREAK REGISTER H - Load pulse for the high byte of the transmit data register. (sheets D4 and D10).

LD CSR HIGH BYTE H - Load pulse for the high byte of the control and status register (sheet D4).

LD CSR LOW BYTE H - Load pulse for the low byte of the control and status register (sheet D4).

LD LPR REGISTER L - Load pulse for the line parameter register (sheets D4 and D8).

LD TCR HIGH BYTE H - Load pulse for the high byte of the transmit control register (sheet D4).

LD TCR LOW BYTE H - Load pulse for the low byte of the transmit control register (sheet D4).

LD TDR REGISTER H - Load pulse for the low byte of the transmit data register (sheet D4).

LINE A, LINE B - Bits 00 and 01 of the line parameter register. This is a 2-bit code that specifies the number of the line to which the parameters apply.

LINE ENAB0 through LINE ENAB3 - Bits 00 through 03 in the transmit control register. Each of these bits enables transmission on the corresponding line.

LOAD IN PROGRESS L - Indicates that either the line parameter register or the transmit data register is being loaded. BRPLY is delayed 300 ns while a load is in progress for either of these two registers (sheet D4).

LOAD SILO H - Enables silo buffers to load data (sheets D11 and D12).

LPR - Line parameter register. Refer to Table 3-4.

MAINT - Maintenance bit (CSR bit 03). Enables the internal loop-back maintenance mode.

MAINTENANCE H - This signal is set by the MAINT bit (sheet D5) and controls the maintenance mode data selector (sheet D10).

MASTER CLEAR H - This signal is derived from the clear bit CLR (CSR bit 04). See sheet D5.

MASTER SCAN CLOCK H - This signal is produced by dividing the master oscillator clock signal (sheet D8). It drives the receiver scanner (sheet D11).

MASTER SCAN ENABLE H - Set by the MSE bit. Enables both transmitter and receiver control circuitry (sheets D5, D9, D11).

MASTER SCAN ENABLE L – Set by the MSE bit. Enables the master scan clock (sheets D5 and D8).

MSE – Master Scan Enable. CSR bit 05.

MSR – Modem Status Register. Refer to Paragraph 3.2.5.

ODD PAR – Odd Parity. Line parameter register bit 07. Refer to Table 3-4.

OR 00 through OR 03 – Overrun error signals from UARTs (sheets D13 and D14) to silo buffer (sheet D12).

OUT HB – Output high byte. Indicates that an output data transfer will be made to the high byte of the selected register (sheet D4).

OUT LB – Output low byte. Indicates that an output data transfer will be made to the low byte of the selected register (sheet D4).

OVRN ERR – Overrun Error. RBUF bit 14. Refer to Table 3-3.

PAR ENAB – Parity Enable. Line parameter register bit 06. Refer to Table 3-4.

PAR ERR – Parity Error. RBUF bit 12. Refer to Table 3-3.

PE 00 through PE 03 – Parity error signals from the UARTs (sheets D13 and D14) to silo the buffer (sheet 12).

PSW – Processor Status Word.

QBUS – LSI-11 Bus.

RBUF – Receiver Buffer. Refer to Table 3-3.

RBUF D0 through RBUF D7 – Received data bits. RBUF bits 0 through 7.

RCV CLOCK 00 H through RCV CLOCK 03 H – Receiver clocks from the baud rate generators (sheet D8) to the UARTs (sheets D13 and D14).

RCV DATA 00 through RCV DATA 03 – Received data bits from the silo buffer (sheet D12) to the multiplexers (sheet D3).

RCV DATA ENABLE 00 through RCV DATA ENABLE 03 – These signals enable the UARTs for the selected lines. They originate in the receiver control circuitry (sheet D11) and go to the UARTs (sheets D13 and D14).

RD1 through RD8 – Received data bits from the UARTs (sheets D13 and D14) to the silo buffer (sheet D12).

RDONE – Receiver Done. CSR bit 07. Refer to Table 3-2.

READ DEVICE H and READ L – These signals control the operating mode of the bus transceivers (sheets D2 and D4).

READ RCV BUFFER H – This signal controls the unloading of the silo buffer (sheets D4 and D12).

RECEIVER DONE H – In the DZV11, this signal does not come from the UARTs. It is the result of anding the Output Ready signals from each of the four FIFO memory chips (sheet 12). It sets the RDONE bit in the CSR (sheet D3) to indicate that a character of received data is ready in the silo buffer.

RECEIVER INTR ENABL – Receiver Interrupt Enable (sheet D5).

RESET DA00 through DA03 – These signals are made up in the receiver control circuitry (sheet D11) to reset the Data Available signals in the UART (sheets D13 and D14) for the selected line.

RI – Ring Indicator.

RI0 through RI3 – Modem status register bits 0 through 3, indicating the states of the Ring signal on the corresponding lines.

RIE – Receiver Interrupt Enable. CSR bit 06. Refer to Table 3-2.

RING 00 through RING 03 – The Ring Indicator signals for lines 0 through 3, after having been converted from EIA to TTL levels (sheet D7).

RO – Read-Only.

RTS – Request to Send. Refer to Table 5-2.

RW – Read/Write.

RX ENAB – Receiver Enable. Line parameter register bit 12. Refer to Table 3-4.

RX LINE A, RX LINE B – Receiver Line A and B, respectively. RBUF bits 08 and 09. Refer to Table 3-3.

SA – Silo Alarm. CSR bit 13. Refer to Table 3-2.

SAE – Silo Alarm Enable. CSR bit 12. Refer to Table 3-2.

SEL 0 – Select line for device register 0 (the CSR). See sheet D4.

SEL 2 – Select line for device register 2. For an input (read) operation, this is the RBUF. For an output (write) operation, this is the LPR. See sheet D4.

SEL 4 – Select line for device register 4 (the TCR). See sheet D4.

SEL 6 – Select line for device register 6. For an input (read) operation, this is the MSR. For an output (write) operation, this is the TDR. See sheet D4.

SERIAL IN00 H through SERIAL IN03 H – Serial input data from each of the four lines. It is called Data In between the receivers (sheet D7) and the maintenance mode data selector (sheet D10). From there to the UARTs (sheets D13 and D14), it is called Serial In.

SERIAL OUT00 through SERIAL OUT03 – Serial data out of the UARTs (sheets D13 and D14). It goes to the EIA drivers and the maintenance mode data selector (sheet D10).

SILO – This term refers to a buffer that automatically shifts data from its input end to its output end. When a silo is loaded, the data does not queue up from the input end toward the output end, as in a shift register. Instead, it stacks up at the output end, and is immediately available for unloading.

SILO ALARM H – This signal is the output of a latch that is set when 16 characters have entered the silo (sheet D11). It is cleared by either reading the RBUF or clearing the Silo Alarm Enable bit in the CSR.

SILO LOAD REQUEST H – This signal is asserted when the Data Available signal for the selected line is set and the In Ready signals from the silo buffer chips are set. See sheet D12.

SPEED CODE A through SPEED CODE D – Bits 08 through 11 of the line parameter register. Refer to Table 3-4.

STOP CODE – Bit 05 of the line parameter register. Refer to Table 3-4.

TBMT – Transmitter Buffer Empty.

TBMT00 through TMBT03 – These are Transmitter Ready signals from the UARTs (sheets D13 and D14) to the transmitter control circuitry (sheet D9).

TBUF0 through TBUF7 – Transmit data bits; bits 0 through 7 of the TDR.

TCR – Transmitter control register. Refer to Paragraph 3.2.4.

TDR – Transmit data register. Refer to Paragraph 3.2.6.

THRL00 L through THRL03 L – Transmitter Holding Register Load signal for lines 0 through 3. From the transmitter control circuitry (sheet D9) to the UARTs (sheets 13 and 14).

TIE – Transmitter Interrupt Enable. CSR bit 14. Refer to Table 3-2.

TLINE A, TLINE B – CSR bits 08 and 09. Indicate which line is selected for transmission. Refer to Table 3-2.

TRAN INTR ENBL H – Transmitter Interrupt Enable signal (sheet D5).

TRANSMITTER READY H – This signal indicates that a line has been selected and that the corresponding UART transmitter is ready to be loaded.

TRDY – Transmitter Ready. CSR bit 15. Refer to Table 3-2.

TTL – Transistor-Transistor Logic. The normal logic levels are approximately 4 V for one state and 0 V for the other.

TX CLOCK 00 H through TX CLOCK 03 H – Transmitter clocks for lines 0 through 3. They come from the baud rate generators (sheet D8) and go to the UARTs (sheets D13 and D14).

UART – Universal Asynchronous Receiver/Transmitter. Refer to Appendix A.

UNLOAD SILO H – The unload signal to the Shift Out pin on the silo buffer memory chips.

VECTOR BIT 02 – Bit 02 of the vector term. This determines whether the computer uses a receiver interrupt service routine or a transmitter interrupt service routine. See sheets D5 and D2.

VECTOR-TO-BUS H – This signal asserts the vector selected by the switch pack at E2 (sheet D5). It also goes to the protocol chip (sheet D4) to cause assertion of BRPLY.

XMIT DATA 00 through XMIT DATA 03 – Transmitted data leaving the EIA drivers.

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